



MOTOROLA

**SN75451BP
SN75452BP
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SN75454BP**

DUAL PERIPHERAL DRIVERS

These versatile devices are useful for interfacing digital logic to industrial electronic systems. They are useful as lamp drivers, relay drivers, logic buffers, line drivers, or MOS drivers.

Each of these devices consists of a pair of M TTL gates with the output of each gate internally connected to the base of a transistor.

- SN75451BP provides the AND function
- SN75452BP provides the NAND function
- SN75453BP provides the OR function
- SN75454BP provides the NOR function

- 300 mA Output Current Capability
- Output Breakdown Voltage – 30 V Min
- M TTL compatible Inputs
- Guaranteed AC Limits

DUAL PERIPHERAL DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

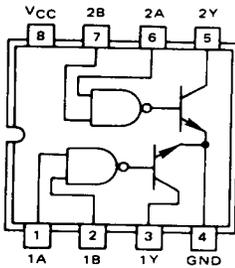


**U SUFFIX
CERAMIC PACKAGE
CASE 693**



**P SUFFIX
PLASTIC PACKAGE
CASE 626**

SN75451BP – Positive AND



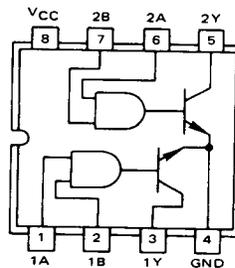
Positive Logic: $Y = AB$

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	H ("off" state)

H = high level, L = low level.

SN75452BP – Positive NAND



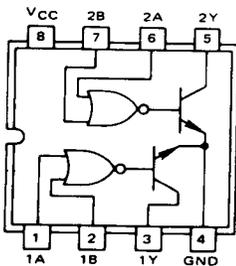
Positive Logic: $Y = \overline{AB}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	L ("on" state)

H = high level, L = low level.

SN75453BP – Positive OR



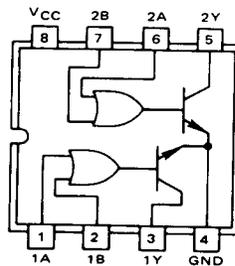
Positive Logic: $Y = A + B$

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	H ("off" state)

H = high level, L = low level.

SN75454BP – Positive NOR



Positive Logic: $Y = \overline{A + B}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	L ("on" state)

H = high level, L = low level.

SN75451BP, SN75452BP, SN75453BP, SN75454BP

MAXIMUM RATINGS (T_A = 0°C to 70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage(1)	V _{CC}	7.0	Vdc
Input Voltage	V _I	5.5	Vdc
Interemitter Voltage(2)	—	5.5	Vdc
Output Voltage(3)	V _O	30	Vdc
Output Current(4)	I _O	300	mA
Power Dissipation @ T _A = 25°C	P _D	830	mW
Derate above T _A = +25°C		6.6	mW/°C
Operating Ambient Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

- (1) Voltage values are with respect to network ground terminal.
- (2) This is the voltage between two emitters of a multiple-emitter transistor.
- (3) This is the maximum voltage which should be applied to any output when it is in the "off" state.
- (4) Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

5

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for 4.75 ≥ V_{CC} ≥ 5.25 V and 0°C ≤ T_A ≤ 70°C)

Characteristic	Figure	Symbol	Min	Typ (1)	Max	Unit
Input Voltage – High Logic State	1,2	V _{IH}	2.0	—	—	Vdc
Input Voltage – Low Logic State	1,2	V _{IL}	—	—	0.8	Vdc
Input Clamp Voltage (V _{CC} = 4.75 V, I _I = -12 mA)	4	V _I	—	-1.2	-1.5	Vdc
Output Current – High Logic State (V _{CC} = 4.75 V, V _{OH} = 30 V, V _{IH} = 2.0 V) (V _{CC} = 4.75 V, V _{OH} = 30 V, V _{IL} = 0.8 V)	2	I _{OH}	—	—	100	μA
Output Voltage – Low Logic State (V _{CC} = 4.75 V, V _{IL} = 0.8 V) (V _{CC} = 4.75 V, V _{IH} = 2.0 V) (I _{OL} = 100 mA) (I _{OL} = 300 mA)	1	V _{OL}	—	0.25 0.5	0.4 0.7	Vdc
Input Current – High Logic State (V _{CC} = 5.25 V, V _I = 2.4 V) (V _{CC} = 5.25 V, V _I = 5.5 V)	3	I _{IH}	—	—	40 1.0	μA mA
Input Current – Low Logic State (V _{CC} = 5.25 V, V _I = 0.4 V)	4	I _{IL}	—	-1.0	-1.6	mA
Power Supply Current – Output High Logic State (V _{CC} = 5.25 V, V _I = 5.0 V) (V _{CC} = 5.25 V, V _I = 0) (V _{CC} = 5.25 V, V _I = 5.0 V) (V _{CC} = 5.25 V, V _I = 0)	5	I _{CC} H	—	7.0 11 8.0 13	11 14 11 17	mA
Power Supply Current – Output Low Logic State (V _{CC} = 5.25 V, V _I = 0) (V _{CC} = 5.25 V, V _I = 5.0 V) (V _{CC} = 5.25 V, V _I = 0) (V _{CC} = 5.25 V, V _I = 5.0 V)	5	I _{CC} L	—	52 56 54 61	65 71 68 79	mA

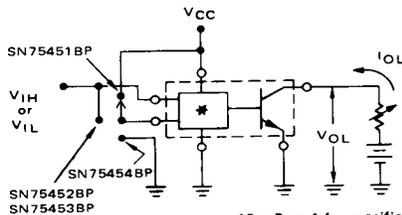
(1) Typical Values Measured with V_{CC} = 5.0 V, T_A = 25°C.

TEST CIRCUITS

(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)

FIGURE 1 – V_{OL}.

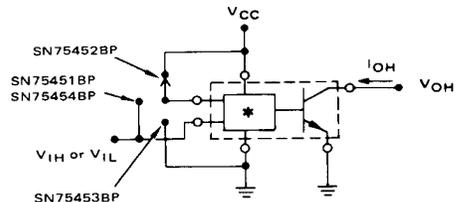
V_{IH} – SN75452BP and SN75454BP
V_{IL} – SN75451BP and SN75453BP



*See Page 1 for specific gate type.

FIGURE 2 – I_{OH}.

V_{IH} – SN75451BP and SN75453BP
V_{IL} – SN75452BP and SN75454BP



Each input is tested separately.

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SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

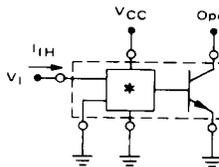
Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time (I _O ≈ 200 mA, C _L = 15 pF, R _L = 50 ohms)						
SN75451BP Low-to-High-Level Output	t _{PLH}	6	—	17	25	ns
SN75451BP High-to-Low-Level Output	t _{PHL}	6	—	18	25	ns
SN75452BP Low-to-High-Level Output	t _{PLH}	6	—	18	35	ns
SN75452BP High-to-Low-Level Output	t _{PHL}	6	—	16	35	ns
SN75453BP Low-to-High-Level Output	t _{PLH}	6	—	15	25	ns
SN75453BP High-to-Low-Level Output	t _{PHL}	6	—	17	25	ns
SN75454BP Low-to-High-Level Output	t _{PLH}	6	—	25	35	ns
SN75454BP High-to-Low-Level Output	t _{PHL}	6	—	19	35	ns
Transition Time (I _O ≈ 200 mA, C _L = 15 pF, R _L = 50 ohms)						
SN75451BP Low-to-High-Level Output	t _{TLH}	6	—	6.0	8.0	ns
SN75451BP High-to-Low-Level Output	t _{THL}	6	—	8.0	12	ns
SN75452BP Low-to-High-Level Output	t _{TLH}	6	—	6.0	8.0	ns
SN75452BP High-to-Low-Level Output	t _{THL}	6	—	9.0	12	ns
SN75453BP Low-to-High-Level Output	t _{TLH}	6	—	5.0	8.0	ns
SN75453BP High-to-Low-Level Output	t _{THL}	6	—	8.0	12	ns
SN75454BP Low-to-High-Level Output	t _{TLH}	6	—	5.0	8.0	ns
SN75454BP High-to-Low-Level Output	t _{THL}	6	—	8.0	12	ns

5

TEST CIRCUITS (Continued)

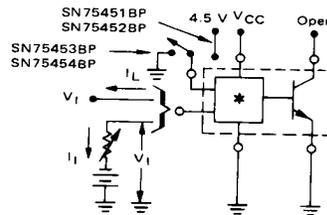
(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)

FIGURE 3 — I_{IH}
(ALL DEVICE TYPES)



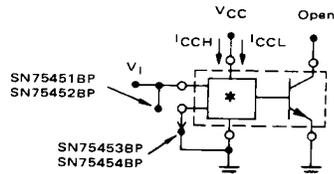
Each input is tested separately.

FIGURE 4 — I_{IL}, V_I
(ALL DEVICE TYPES)



Each input is tested separately.

FIGURE 5 — I_{CCH}, I_{CCL}
(ALL DEVICE TYPES)

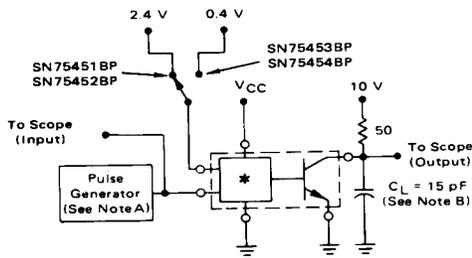


Both gates are tested simultaneously.

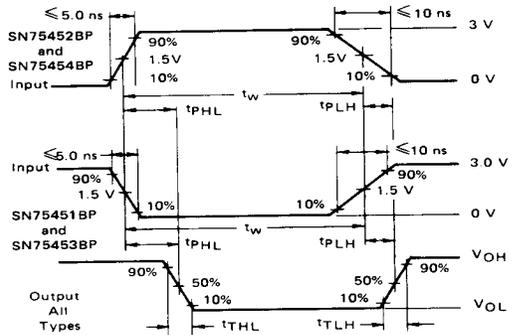
*See page 1 for specific gate type.

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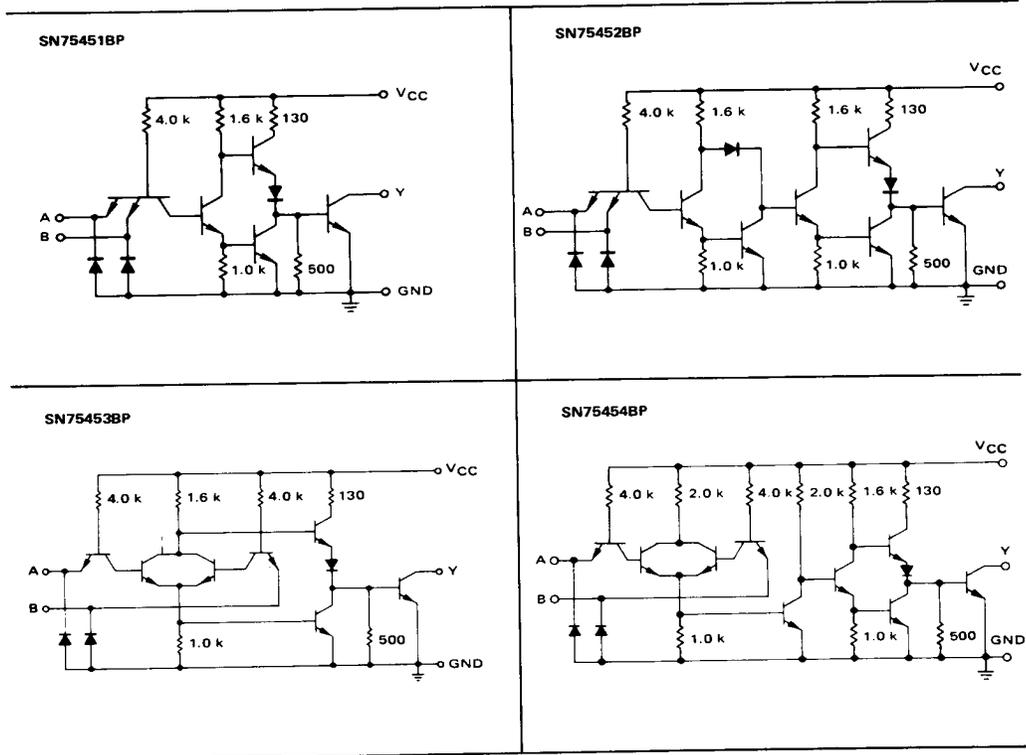
FIGURE 6 - SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



NOTES: A. Pulse generator characteristics: $t_w = 0.5 \mu s$,
 PRR = 1.0 MHz, $z_o \approx 50 \Omega$
 B. C_L includes probe and test fixture capacitance.



REPRESENTATIVE SCHEMATIC DIAGRAMS (1/2 Circuits Shown)



5