

# PCM1740

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## *SoundPLUS*™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER with VCXO and PLL

### FEATURES

**COMPLETE DELTA-SIGMA STEREO DAC**  
**VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR: 27MHz ±150ppm Output with 0V to 3V Input**  
**PROGRAMMABLE PLL**  
**256f<sub>s</sub> or 384f<sub>s</sub> Audio System Clock Output**  
**DYNAMIC PERFORMANCE:**  
**Dynamic Range: 94dB**  
**SNR: 94dB**  
**THD+N: 89dB**  
**SAMPLING FREQUENCIES:**  
**16kHz, 22.05kHz, 24kHz**  
**32kHz, 44.1kHz, 48kHz**  
**64kHz, 88.2kHz, 96kHz**  
**SERIAL AUDIO INTERFACE:**  
**Standard or I<sup>2</sup>S Data Formats**  
**16-, 20-, or 24-Bit Data**  
**I<sup>2</sup>C-BUS™ INTERFACE FOR CONTROL REGISTERS<sup>(1)</sup>:**  
**Slave Receiver Operation**  
**7-Bit Addressing**  
**Standard Transfer Rate (up to 100kbps)**  
**PROGRAMMABLE CONTROLS:**  
**Digital Attenuation (256 steps)**  
**Soft Mute**  
**Infinite Zero Detect Mute**  
**De-Emphasis (32kHz, 44.1kHz, 48kHz)**  
**DAC Output Mode**  
**SINGLE +5V SUPPLY**  
**SMALL SSOP-24 PACKAGE**

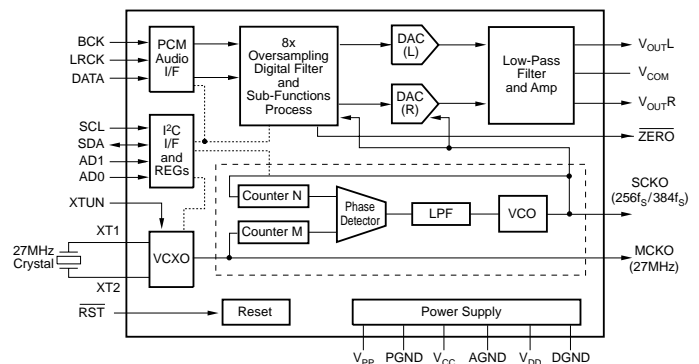
### DESCRIPTION

The PCM1740 is a complete stereo audio digital-to-analog converter with on-chip PLL and VCXO. The PCM1740 is designed specifically for set-top box applications requiring high-quality audio playback, a precision tuned 27MHz master clock source, and support for multiple audio-sampling frequencies.

The stereo D/A converter utilizes multi-bit, delta-sigma architecture, which includes an 8x interpolation filter, third-order noise shaping, 5-level amplitude quantization, and an analog low-pass filter. The PCM1740 includes a number of user-programmable functions, which are accessed via a standard I<sup>2</sup>C-Bus interface.

### APPLICATIONS

**SET-TOP BOXES**  
**DIGITAL BROADCAST RECEIVERS**



NOTE: (1) I<sup>2</sup>C-Bus™ is a registered trademark of Philips Semiconductor.

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# SPECIFICATIONS

All specifications at  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{DD} = V_{PP} = 5.0\text{V}$ ,  $f_S = 44.1\text{kHz}$ , system clock =  $384f_S$ , 16-bit data, unless otherwise noted.

| PARAMETER   | CONDITIONS                                | PCM1740E  |           |      | UNITS         |
|---|---|---|-----------|------|---------------|
|   |   | MIN   | TYP       | MAX  |               |
| <b>RESOLUTION</b>   |   | 16  |           |      | Bits          |
| <b>DATA FORMAT</b>  |   | Standard/I <sup>2</sup> S Selectable<br>16/20/24 Selectable<br>MSB First, Two's Binary Complement |           |      | Bits          |
| Audio Interface Format                                      |   |   |           |      |               |
| Audio Data Bit Length                                       |   |   |           |      |               |
| Audio Data Format   |   |   |           |      |               |
| Sampling Frequency ( $f_S$ )                                | Standard ( $f_S$ )                        | 32  | 44.1      | 48   | kHz           |
|   | Half ( $f_S$ )                            | 16  | 22.05     | 24   | kHz           |
|   | Double ( $f_S$ )                          | 64  | 88.2      | 96   | kHz           |
| Internal System Clock Frequency                             |   | $256f_S/384f_S$   |           |      |               |
| <b>DIGITAL INPUT/OUTPUT</b>                                 |   | TTL Compatible  |           |      |               |
| Logic Family  | Input Logic                               | 2.0   |           |      | VDC           |
| High Level Input Voltage: $V_{IH}^{(1), (2)}$               |   |   |           |      | VDC           |
| Low Level Input Voltage: $V_{IL}^{(1), (2)}$                |   |   |           |      | $\mu\text{A}$ |
| High Level Input Current: $I_{IH}^{(1), (2)}$               | $V_{IH} = V_{DD}$                         |   |           |      | $\mu\text{A}$ |
| Low Level Input Current:                                    |   |   |           |      | $\mu\text{A}$ |
| $I_{IL}^{(1)}$  | $V_{IL} = 0\text{V}$                      |   |           |      | $\mu\text{A}$ |
| $I_{IL}^{(2)}$  | $V_{IL} = 0\text{V}$                      |   |           |      | VDC           |
| High Level Output Voltage: $V_{OH}^{(3)}$                   | $I_{OH} = -2\text{mA}$                    | $V_{DD} - 0.5\text{V}$  |           |      | VDC           |
| Low Level Output Voltage:                                   |   |   |           |      | VDC           |
| $V_{OH}^{(3)}$  | $I_{OL} = 4\text{mA}$                     |   |           |      | VDC           |
| $V_{OL}^{(4)}$  | $I_{OL} = 2\text{mA}$                     |   |           |      | VDC           |
| <b>DIGITAL INPUT/OUTPUT of I<sup>2</sup>C-BUS INTERFACE</b> |   |   |           |      |               |
| High Level Input Voltage: $V_{IH}^{(5)}$                    |   | 3.0   |           |      | V             |
| Low Level Input Voltage: $V_{IL}^{(5)}$                     |   | -0.3  | 1.5       |      | V             |
| Low Level Output Voltage: $V_{OL}^{(6)}$                    |   | 0   | 0.4       |      | V             |
| Output Fall Time: $t_{OF}^{(7)}$                            |   |   | 250       |      | ns            |
| Input Logic Current: $I_I^{(8)}$                            | 10% to 90% of $V_{DD}$                    | -10   | 10        |      | $\mu\text{A}$ |
| Capacitance for each I/O pin: $C_I^{(5)}$                   |   |   | 10        |      | pF            |
| <b>VCXO CHARACTERISTICS (MCKO)</b>                          | 27MHz, Fundamental Crystal                |   |           |      |               |
| Crystal Clock Frequency <sup>(9)</sup>                      |   |   | 27.0000   |      | MHz           |
| Crystal Clock Accuracy <sup>(9)</sup>                       |   |   | $\pm 30$  |      | ppm           |
| XTUN Tuning Voltage Range <sup>(10)</sup>                   |   | 0   | 60        | 3.0  | V             |
| XTUN Input Impedance <sup>(10)</sup>                        |   |   | 27.0000   |      | k $\Omega$    |
| Output Clock Frequency                                      | XTUN = 1.3V                               |   | 27.0000   |      | MHz           |
| Output Clock Accuracy                                       | XTUN = 1.3V                               |   | $\pm 50$  |      | ppm           |
| VCXO Tuning Range   | XTUN = 0V - 3V                            |   | 300       |      | ppm           |
| Output Clock Duty Cycle                                     | 10pF Load                                 | 35  | 45        | 55   | %             |
| Output Clock Jitter   | Standard Deviation                        |   | 100       |      | ps            |
| Output Rise Time  | 20% to 80% $V_{DD}$ , 10pF Load           |   | 4         |      | ns            |
| Output Fall Time  | 80% to 20% $V_{DD}$ , 10pF Load           |   | 4         |      | ns            |
| Response Time <sup>(11)</sup>                               |   |   |           | 10   | $\mu\text{s}$ |
| Power Up Time <sup>(12)</sup>                               |   |   |           | 5    | ms            |
| <b>PLL AC CHARACTERISTICS (SCKO)</b>                        |   |   |           |      |               |
| Output Clock Frequency                                      | MCKO = 27.0MHz                            | 4.096   | 36.864    |      | MHz           |
| Output Clock Duty Cycle                                     | 10pF Load                                 | 40  | 50        | 60   | %             |
| Output Clock Jitter   | Standard Deviation                        |   | 150       |      | ps            |
| Output Rise Time  | 20% to 80% $V_{DD}$ , 10pF Load           |   | 4         |      | ns            |
| Output Fall Time  | 80% to 20% $V_{DD}$ , 10pF Load           |   | 4         |      | ns            |
| Frequency Transition Time <sup>(13)</sup>                   |   |   |           | 20   | ms            |
| Power Up Time <sup>(14)</sup>                               |   |   | 15        | 30   | ms            |
| <b>DYNAMIC PERFORMANCE<sup>(15)</sup></b>                   |   |   |           |      |               |
| THD+N:  |   |   |           |      |               |
| $V_{OUT} = 0\text{dB}$                                      | $f_S = 44.1\text{kHz}$                    |   | 0.0035    | 0.01 | %             |
|   | $f_S = 96\text{kHz}$                      |   | 0.007     |      | %             |
| $V_{OUT} = -60\text{dB}$                                    | $f_S = 44.1\text{kHz}$                    |   | 0.0035    | 0.01 | %             |
|   | $f_S = 96\text{kHz}$                      |   | 0.007     |      | %             |
| Dynamic Range   | $f_S = 44.1\text{kHz}$ , EIAJ, A-Weighted | 90  | 94        |      | dB            |
|   | $f_S = 96\text{kHz}$ , A-Weighted         |   | 90        |      | dB            |
| Signal-to-Noise Ratio <sup>(16)</sup>                       | $f_S = 44.1\text{kHz}$ , EIAJ, A-weighted | 90  | 94        |      | dB            |
|   | $f_S = 96\text{kHz}$ , A-weighted         |   | 90        |      | dB            |
| Channel Separation  | $f_S = 44.1\text{kHz}$                    | 88  | 92        |      | dB            |
|   | $f_S = 96\text{kHz}$                      |   | 88        |      | dB            |
| Level Linearity Error                                       | $V_{OUT} = -90\text{dB}$                  |   | $\pm 1.0$ |      | dB            |

# SPECIFICATIONS

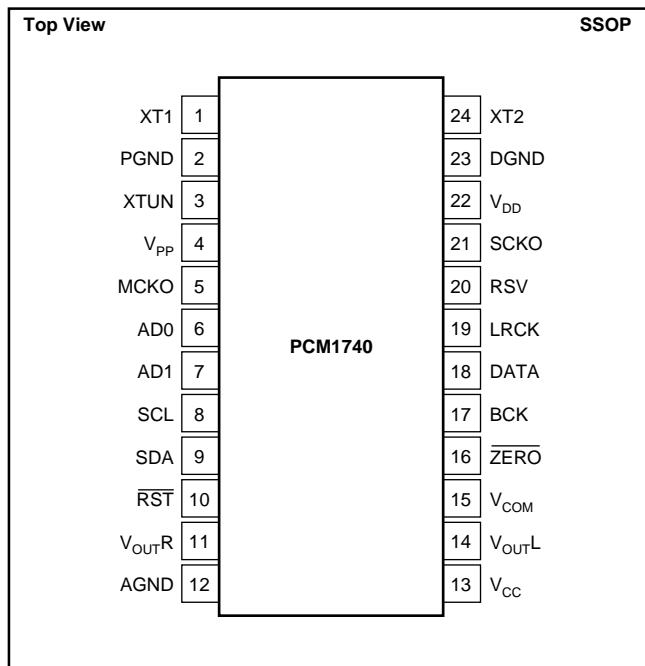
All specifications at  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{DD} = V_{PP} = 5.0\text{V}$ ,  $f_S = 44.1\text{kHz}$ , system clock =  $384f_S$ , 16-bit data, unless otherwise noted.

| PARAMETER   | CONDITIONS   | PCM1740E       |                                     |                                      | UNITS  |
|---|--|----------------|-------------------------------------|--------------------------------------|--|
|   |  | MIN            | TYP                                 | MAX                                  |  |
| <b>DC ACCURACY</b><br>Gain Error<br>Gain Mismatch, Channel-to-Channel<br>Bipolar Zero Error   |  |                | $\pm 1.0$<br>$\pm 1.0$<br>$\pm 1.0$ | $\pm 3.0$<br>$\pm 3.0$               | % of FSR<br>% of FSR<br>% of FSR                           |
| <b>ANALOG OUTPUT</b><br>Voltage Range<br>Center Voltage<br>Load Impedance   | Full Scale (0dB)<br><br>AC Coupled   |                | $0.62 V_{CC}$<br>$0.5 V_{CC}$       |                                      | Vp-p<br>VDC<br>k $\Omega$                                  |
| <b>DIGITAL FILTER PERFORMANCE</b><br>Passband<br>Stopband<br>Passband Ripple<br>Stopband Attenuation<br>De-Emphasis Error<br>Delay Time |  | $0.555 f_S$    |                                     | $0.445 f_S$<br>$\pm 0.17$<br>$+0.55$ | Hz<br>Hz<br>dB<br>dB<br>dB<br>sec                          |
| <b>ANALOG FILTER PERFORMANCE</b><br>Frequency Response  | 20Hz to 20kHz<br>20Hz to 40kHz   |                | $-0.16$<br>$-0.6$                   |                                      | dB<br>dB   |
| <b>POWER SUPPLY REQUIREMENTS</b><br>Voltage Range<br>Supply Current, $I_{DD} + I_{CC} + I_{PP}$<br>Power Dissipation                    | $V_{DD}, V_{CC}, V_{PP}$<br>$V_{DD} = V_{CC} = V_{PP} = +5\text{V}$<br>$V_{DD} = V_{CC} = V_{PP} = +5\text{V}$ | +4.5           | +5<br>25<br>125                     | +5.5<br>30<br>150                    | VDC<br>mA<br>mW  |
| <b>TEMPERATURE RANGE</b><br>Operation<br>Storage<br>Thermal Resistance, $\theta_{JA}$   |  | $-25$<br>$-55$ |                                     | +85<br>+125                          | $^\circ\text{C}$<br>$^\circ\text{C}$<br>$^\circ\text{C/W}$ |

NOTES: (1) Pins 6, 7, 18, 19: AD0, AD1, BCK, DATA, LRCK (Schmitt trigger input). (2) Pin 10:  $\overline{\text{RST}}$  (Schmitt trigger input with internal pull-up resistor). (3) Pins 5, 21: MCKO, SCKO. (4) Pin 16:  $\overline{\text{ZERO}}$  (open drain output). (5) Pins 8, 9: SCL, SDA. (6) Pin 9: SDA (open drain output,  $I_{OL} = 3\text{mA}$ ). (7) Pin 9: SDA (from  $V_{IHMIN}$  to  $V_{ILMAX}$  with a bus capacitance from 10pF to 400pF). (8) Pins 8, 9: SCL, SDA (input current each I/O pin with an input voltage between  $0.1V_{DD}$  and  $0.9V_{DD}$ ). (9) This characteristic is the requirement for crystal oscillator. (10) Pin 3: XTUN. (11) The maximum response time when the XTUN is changed. (12) The maximum delay time from power on to oscillation. (13) The maximum lock up time when the PLL frequency is changed. (14) The maximum delay time from power on to lock up. (15) Dynamic performance specifications are tested with a 20kHz low-pass filter using a Shibasoku distortion analyzer 725 $^\circ\text{C}$  with 30kHz LPF, 400Hz HPF, Average-Mode. (16) SNR is tested with infinite zero detection circuit disabled.

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## PIN CONFIGURATION



## PIN ASSIGNMENTS

| PIN | NAME              | I/O    | FUNCTION  |
|-----|-------------------|--------|---|
| 1   | XT1               | —      | 27MHz Crystal connection.   |
| 2   | PGND              | —      | PLL and VCXO ground.  |
| 3   | XTUN              | IN     | VCXO tune, tuning voltage range from 0V to 3V.  |
| 4   | V <sub>PP</sub>   | —      | PLL and VCXO power supply, +5V.   |
| 5   | MCKO              | OUT    | Buffered clock output of VCXO.  |
| 6   | AD0               | IN     | Device address pin for I <sup>2</sup> C-BUS. <sup>(1)</sup>                             |
| 7   | AD1               | IN     | Device address pin for I <sup>2</sup> C-BUS. <sup>(1)</sup>                             |
| 8   | SCL               | IN     | Bit clock input for I <sup>2</sup> C-BUS interface.                                     |
| 9   | SDA               | IN/OUT | Serial data for I <sup>2</sup> C-BUS interface.   |
| 10  | RST               | IN     | Reset, active LOW. <sup>(2)</sup>   |
| 11  | V <sub>OUTR</sub> | OUT    | Right-channel analog voltage output.  |
| 12  | AGND              | —      | Analog ground.  |
| 13  | V <sub>CC</sub>   | —      | Analog power supply, +5V.   |
| 14  | V <sub>OUTL</sub> | OUT    | Left-channel analog voltage output.   |
| 15  | V <sub>COM</sub>  | —      | DC common-mode voltage output.  |
| 16  | ZERO              | OUT    | Zero flag output, active LOW. <sup>(3)</sup>  |
| 17  | BCK               | IN     | Bit clock input for serial audio data. <sup>(1)</sup>                                   |
| 18  | DATA              | IN     | Serial audio data input. <sup>(1)</sup>   |
| 19  | LRCK              | IN     | Left and right word clock, equal to the sampling rate (f <sub>s</sub> ). <sup>(1)</sup> |
| 20  | RSV               | —      | Reserved must be open.  |
| 21  | SCKO              | OUT    | System clock output, 256/384 f <sub>s</sub> .   |
| 22  | V <sub>DD</sub>   | —      | Digital power supply, +5V.  |
| 23  | DGND              | —      | Digital ground.   |
| 24  | XT2               | —      | 27MHz Crystal connection.   |

NOTES: (1) Schmitt trigger input. (2) Schmitt trigger input with internal pull-up resistor. (3) Open drain output.

## ABSOLUTE MAXIMUM RATINGS

|  |                                   |
|--|-----------------------------------|
| Power Supply Voltage <sup>(1)</sup> .....        | +6.5V                             |
| Supply Voltage Differences <sup>(2)</sup> .....  | ±0.1V                             |
| GND Voltage Differences <sup>(3)</sup> .....     | ±0.1V                             |
| Digital Input Voltage .....                      | -0.3V to (V <sub>DD</sub> + 0.3V) |
| Analog Input Voltage .....                       | -0.3V to (V <sub>CC</sub> + 0.3V) |
| Input Current (any pins except supplies) .....   | ±10mA                             |
| Operating Temperature Range .....                | -25°C to +85°C                    |
| Storage Temperature .....                        | -55°C to +125°C                   |
| Junction Temperature .....                       | +150°C                            |
| Lead Temperature (soldering, 5s) .....           | +260°C                            |
| Package Temperature (IR reflow, peak, 10s) ..... | +235°C                            |

NOTES: (1) V<sub>CC</sub>, V<sub>DD</sub>, V<sub>PP</sub>. (2) Among V<sub>CC</sub>, V<sub>DD</sub>, V<sub>PP</sub>. (3) Among AGND, DGND, and PGND. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

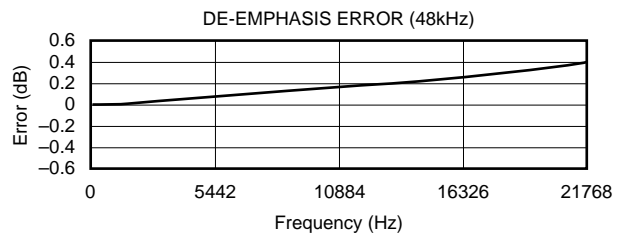
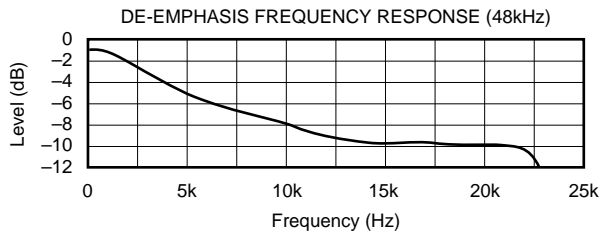
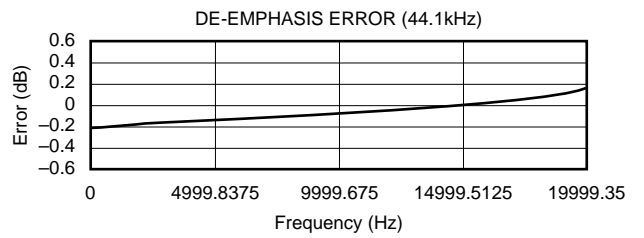
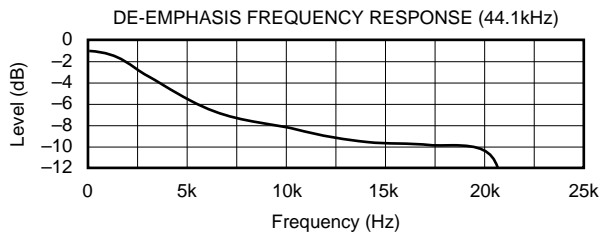
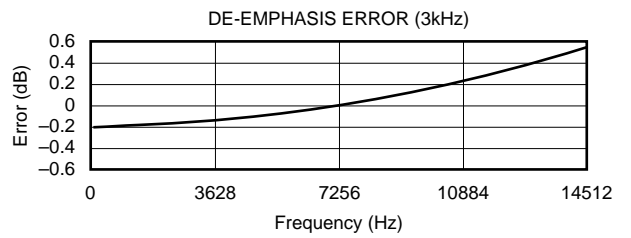
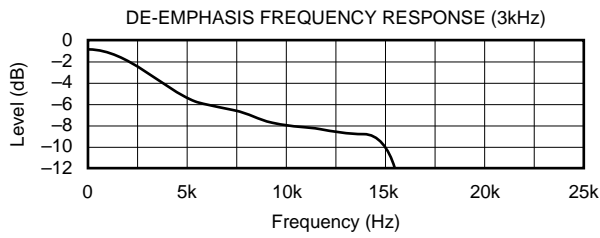
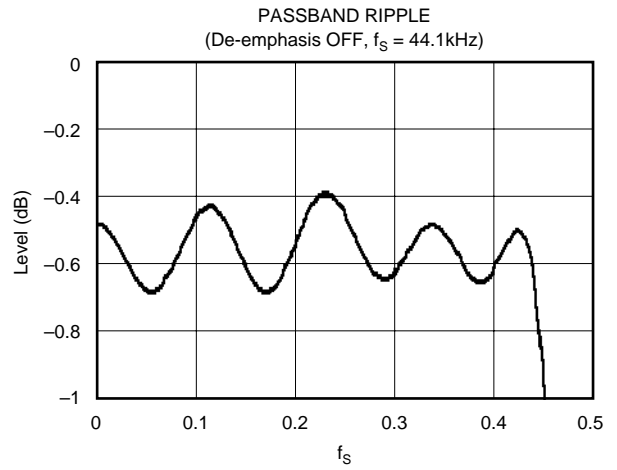
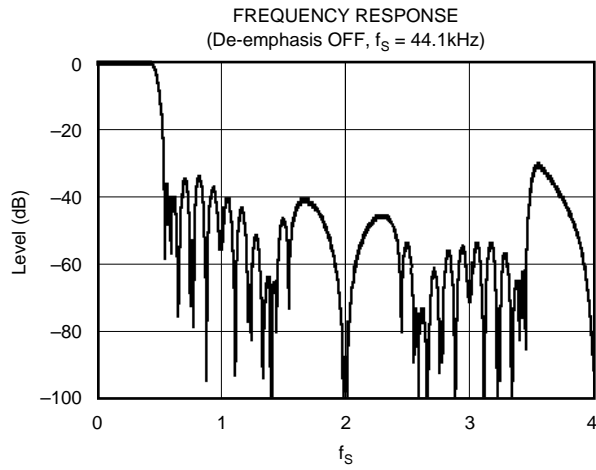
## PACKAGE/ORDERING INFORMATION

| PRODUCT  | PACKAGE | PACKAGE DRAWING NUMBER | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER <sup>(1)</sup> | TRANSPORT MEDIA |
|----------|---------|------------------------|-----------------------------|-----------------|--------------------------------|-----------------|
| PCM1740E | SSOP-24 | 338                    | -25°C to +85°C              | PCM1740E        | PCM1740E                       | Rails           |
| "        | "       | "                      | "                           | PCM1740E        | PCM1740E/2K                    | Tape and Reel   |

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "PCM1740E/2K" will get a single 2000-piece Tape and Reel.

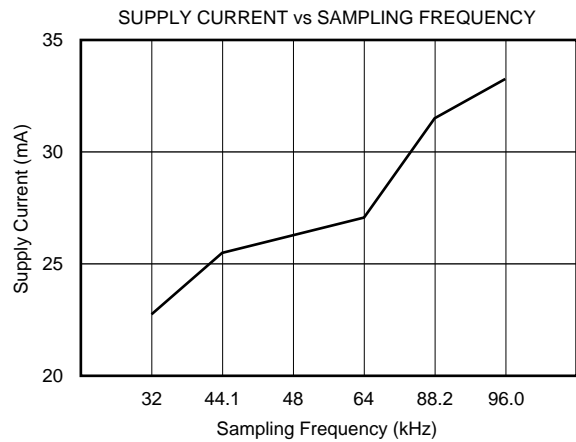
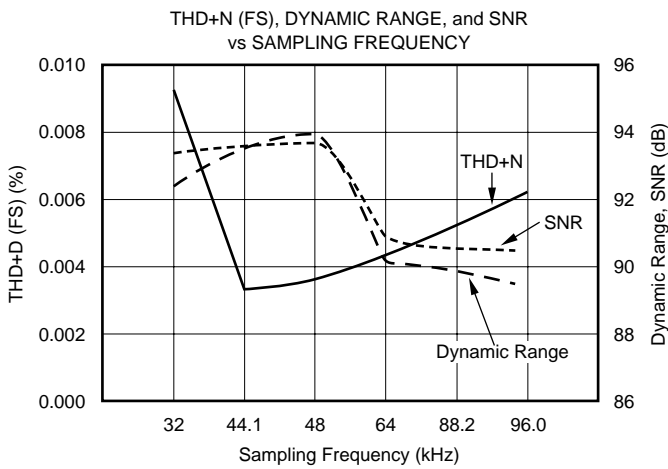
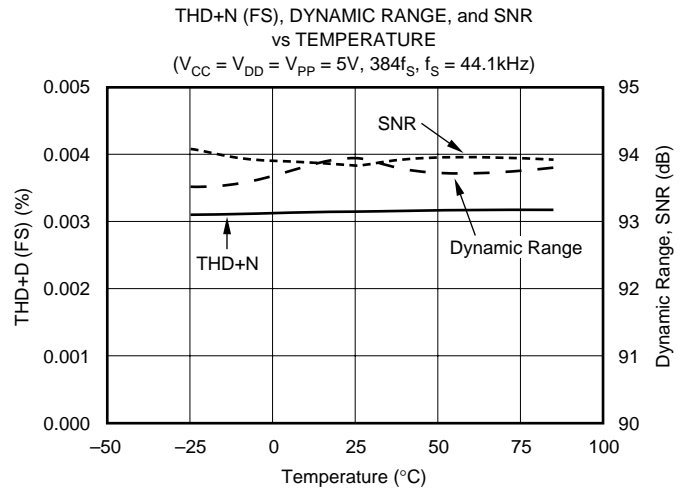
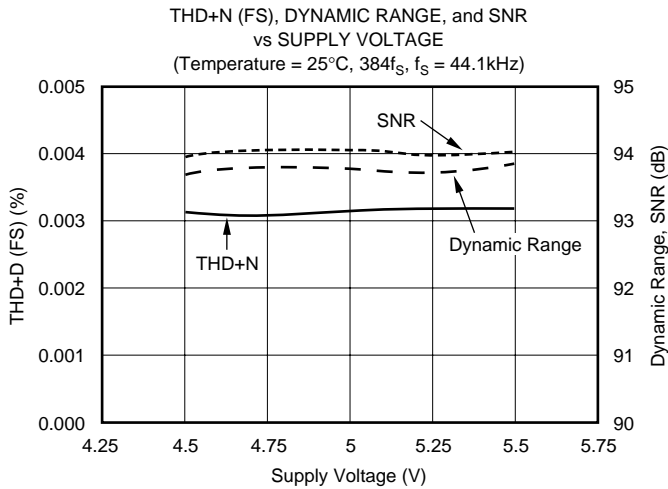
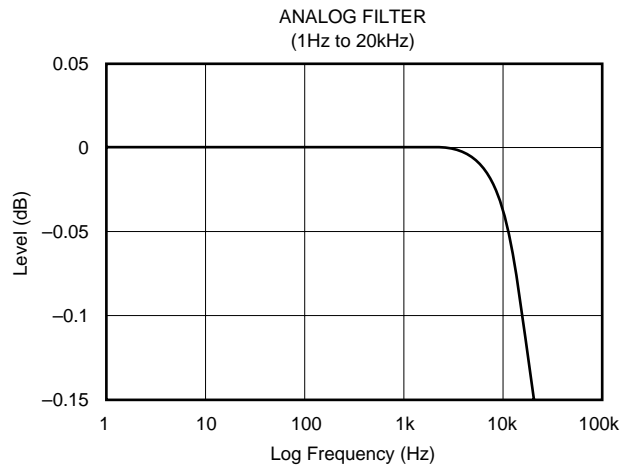
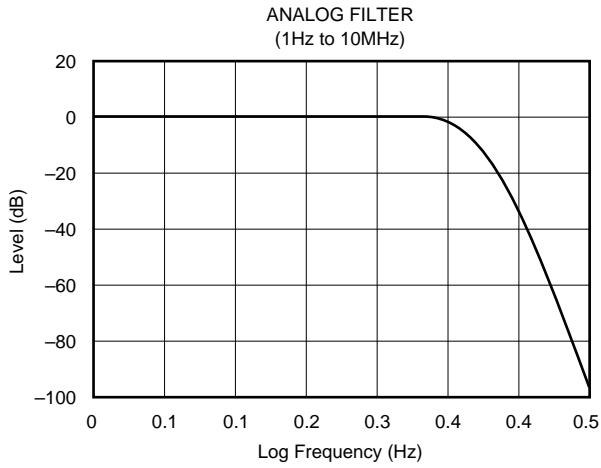
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{DD} = +5\text{V}$ ,  $f_S = 44.1\text{kHz}$ ,  $F_{SCKO} = 384f_S = 16.9344\text{MHz}$ , and 16-bit data, unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{DD} = +5\text{V}$ ,  $f_S = 44.1\text{kHz}$ ,  $F_{SCKO} = 384f_S = 16.9344\text{MHz}$ , and 16-bit data, unless otherwise noted.



# STEREO DIGITAL-TO-ANALOG CONVERTER

The stereo D/A converters of the PCM1740 utilize a multi-level delta-sigma architecture. Based upon a third-order noise shaper and a 5-level amplitude quantizer, this section converts the 8x oversampled, 18-bit input data from the interpolation filter to a 5-level delta-sigma format. A block diagram of the multi-level delta-sigma modulator is shown in Figure 1. This architecture has the advantage of improved stability and increased tolerance to clock jitter when compared to the one-bit (2-level) delta-sigma D/A converters.

The combined oversampling rate of the delta-sigma modulator and the 8x interpolation filter is  $48f_s$  for a  $384f_s$  system clock, and  $64f_s$  for a  $256f_s$  system clock. The theoretical quantization noise performance for the 5-level delta-sigma modulator is shown in Figure 2.

The output of the delta-sigma modulator is low-pass filtered and buffered by an on-chip output amplifier. For best performance, an external low-pass filter is recommended. Refer to the “Applications Information” section of this data sheet for details regarding DAC output filter recommendations.

The PCM1740 includes two analog outputs,  $V_{OUTL}$  (pin 14) and  $V_{OUTR}$  (pin 11), corresponding to the left and right audio outputs. The full-scale output amplitude is  $0.62 \cdot V_{CC}$ , or 3.1Vp-p with a +5V supply and an AC coupled load of 5k $\Omega$  or greater. The analog outputs are centered about the DC common mode voltage, which is typically  $V_{CC}/2$ .

The DC common-mode voltage is made available at the  $V_{COM}$  output (pin 15). This is an unbuffered output, prima-

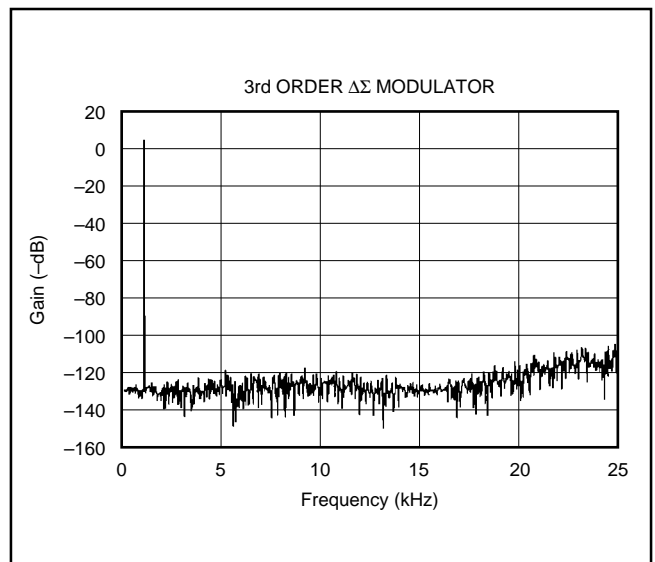


FIGURE 2. Quantization Noise Spectrum.

rily used for de-coupling purposes. See the “Applications Information” section of this data sheet for more information regarding the use of the  $V_{COM}$  output for biasing external circuitry.

## VOLTAGE CONTROLLED CRYSTAL OSCILLATOR (VCXO)

The PCM1740 includes an on-chip voltage-controlled crystal oscillator, or VCXO, which is used to generate the 27MHz master clock required by most digital broadcast and MPEG-2 decoding applications.

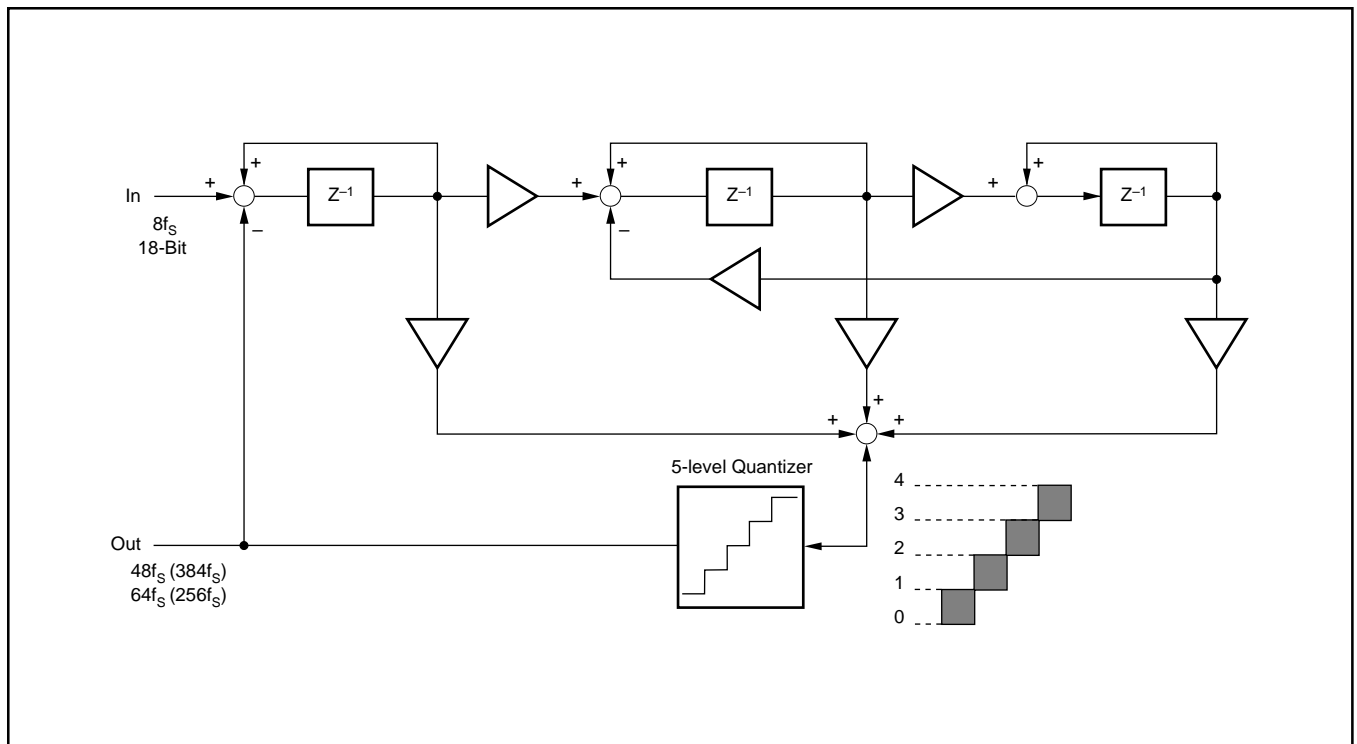


FIGURE 1. 5-Level  $\Delta\Sigma$  Modulator Block Diagram.

The 27MHz clock is available at the MCKO output (pin 5). The VCXO output frequency can be precisely tuned using a control voltage at the XTUN input (pin 3). The tuning range is 27MHz  $\pm$ 150ppm typical for a 0V to +3V control voltage range. Figure 3 shows the VCXO equivalent circuit, while Figure 4 shows the typical tuning curve.

At power up, the VCXO requires 5ms start up time. The VCXO also exhibits a 10 $\mu$ s settling time in response to changes in the XTUN control voltage. VCXO operation and the MCKO output are not effected by the power on or external reset functions, continuing to operate during the initialization sequence.

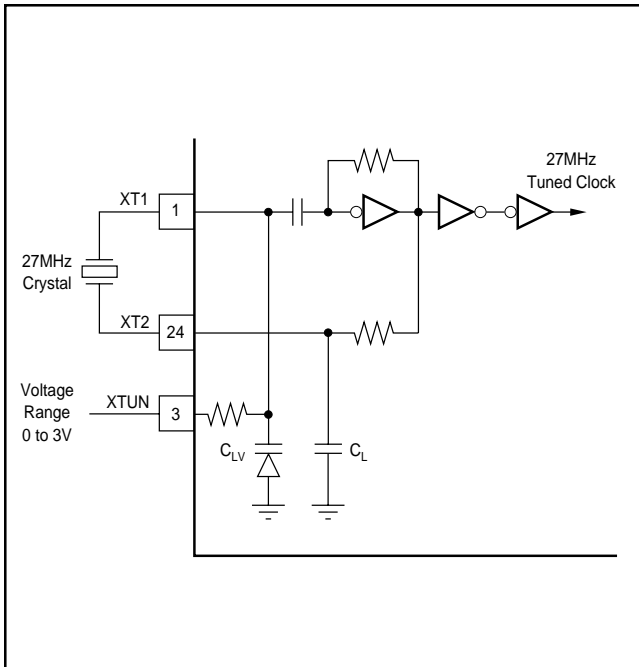


FIGURE 3. VCXO Equivalent Circuit.

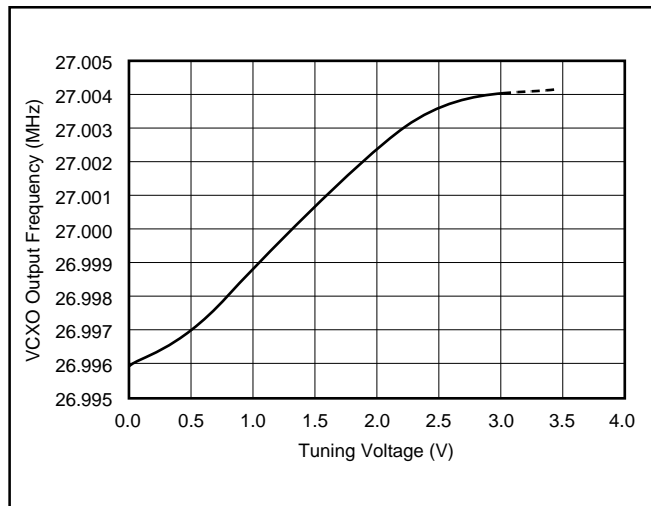


FIGURE 4. VCXO Output Frequency (MCKO) versus Tuning Voltage (XTUN).

### Crystal Selection

The VCXO connects to an external 27MHz crystal via XT1 (pin 1) and XT2 (pin 24). The crystal should be AT-cut, fundamental mode with  $\pm$ 30ppm accuracy and less than 50 $\Omega$  motional resistance. Crystal shunt capacitance should be 3pF maximum, while load capacitance should be less than 7pF. Miniature lead type or surface-mount devices are recommended. External load capacitors are not needed, since they are provided on-chip. The crystal should be placed as close as possible to the XT1 and XT2 pins to reduce effects of parasitic capacitance and land resistance.

### PROGRAMMABLE PHASE LOCKED LOOP (PLL)

The PCM1740 includes an on-chip PLL for generating a 256f<sub>s</sub> or 384f<sub>s</sub> audio system clock from the 27MHz VCXO output. A block diagram of the PLL section is shown in Figure 5. The PLL output clock is used by the digital filter and delta-sigma modulator circuitry, and is made available at the SCKO output (pin 21) for use with additional audio converters and signal processors.

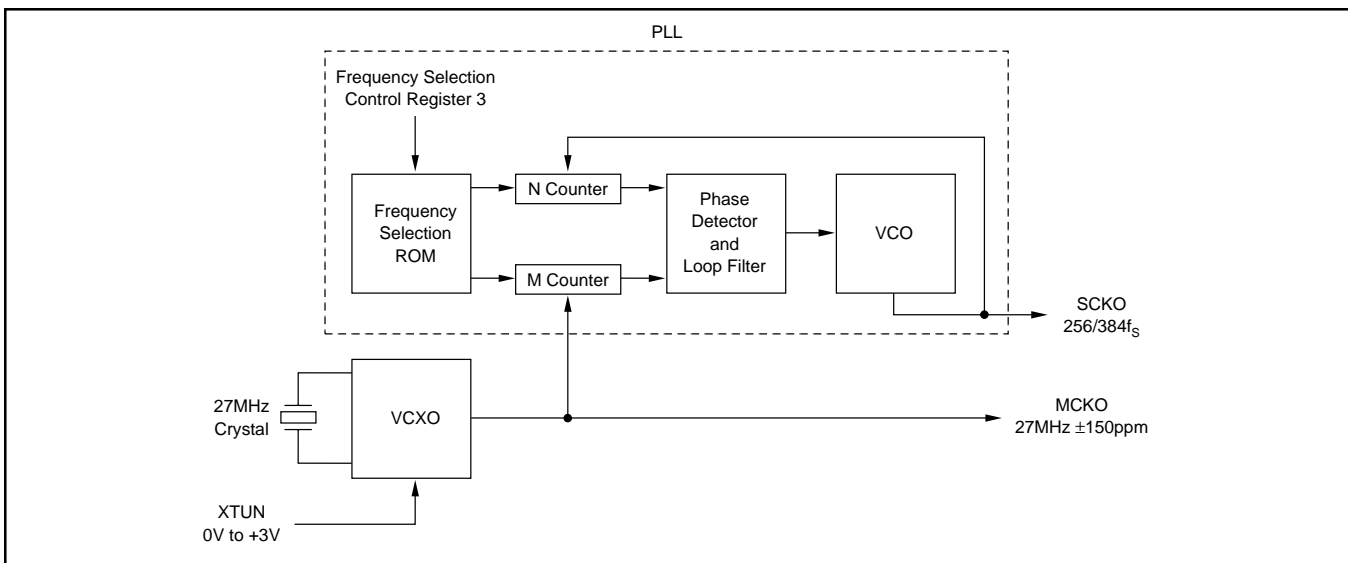


FIGURE 5. PLL Block Diagram.



The PLL can generate one of nine pre-programmed system clock rates for either  $256f_s$  or  $384f_s$  output. The PLL output and sampling frequencies are programmed using Control Register 3. Table I shows the available sampling frequencies and the corresponding PLL output clock rates. The reset default condition for the PLL is  $f_s = 44.1\text{kHz}$  with  $\text{SCKO} = 384f_s$ , or  $16.9344\text{MHz}$ .

At power up, the PLL requires 30ms start up time for stabilization. The PLL also exhibits a settling time of 20ms in response to changes in sampling frequency selection. The PLL output continues to operate during power on or external reset sequences, with the sampling frequency set to  $f_s = 44.1\text{kHz}$  and  $\text{SCKO} = 384f_s$ .

| SAMPLING FREQUENCY (LRCK) |        | INTERNAL SYSTEM Clock - $256f_s$ | INTERNAL SYSTEM Clock - $384f_s$ |
|---------------------------|--------|----------------------------------|----------------------------------|
| 16kHz                     | Half   | 4.096MHz                         | 6.144MHz                         |
| 32kHz                     | Normal | 8.192MHz                         | 12.288MHz                        |
| 64kHz                     | Double | 16.384MHz                        | 24.576MHz                        |
| 22.05kHz                  | Half   | 5.6448MHz                        | 8.4672MHz                        |
| 44.1kHz                   | Normal | 11.2896MHz                       | 16.9344MHz                       |
| 88.2kHz                   | Double | 22.5792MHz                       | 33.8688MHz                       |
| 24kHz                     | Half   | 6.144MHz                         | 9.216MHz                         |
| 48kHz                     | Normal | 12.288MHz                        | 18.432MHz                        |
| 96kHz                     | Double | 24.576MHz                        | 36.864MHz                        |

TABLE I. PLL Sampling and System Clock Frequencies.

## RESET OPERATION

### POWER ON RESET

The PCM1740 includes power-on reset circuitry for start up initialization. The initialization sequence starts when  $V_{DD}$  exceeds 2.2V (typical). The initialization sequence requires 1024 PLL output (or SCKO) clock cycles for completion. During initialization, both  $V_{OUTL}$  and  $V_{OUTR}$  are forced to  $V_{CC}/2$ . Figure 6 shows the power on reset timing, while Table II shows the reset default settings for user-programmable functions. The user should not attempt to write control registers via the I<sup>2</sup>C-Bus interface during the initialization sequence.

### EXTERNAL RESET

The PCM1740 includes an external reset input,  $\overline{\text{RST}}$  (pin 10). This input may be used to force an initialization sequence. As shown in Figure 7, the  $\overline{\text{RST}}$  pin must be held low for a minimum of 20ns. The initialization sequence will then start on the rising edge of  $\overline{\text{RST}}$ . Initialization requires 1024 PLL output (or SCKO) clock cycles for completion. During initialization, both  $V_{OUTL}$  and  $V_{OUTR}$  are forced to  $V_{CC}/2$ . Table II shows the reset default settings for user-programmable functions. The user should not attempt to write control registers via the I<sup>2</sup>C-Bus interface during the initialization sequence.

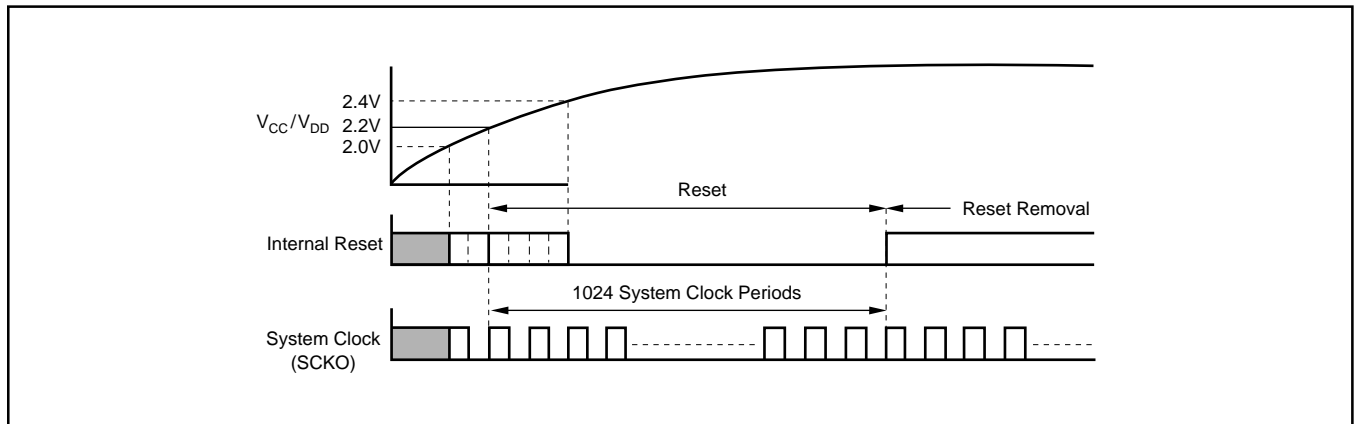


FIGURE 6. Power-On Reset Operation.

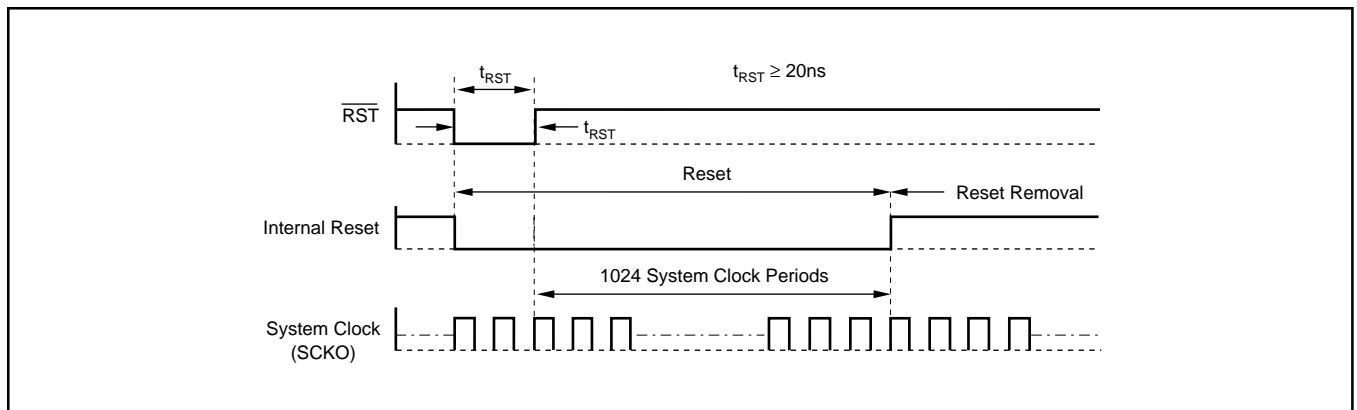


FIGURE 7. External Reset Operation.

## ZERO FLAG OUTPUT

The PCM1740 includes a zero flag output,  $\overline{\text{ZERO}}$  (pin 16). This is an open-drain output, and a 10k $\Omega$  pull-up resistor connected to  $V_{DD}$  is recommended when using the  $\overline{\text{ZERO}}$  flag as a logic output.

The PCM1740 includes an infinite zero detection function that monitors the audio data at the DATA input (pin 18). If the audio data for both the left and right channels is all zeros for 65,536 continuous BCK clock cycles, the zero flag will be activated, turning on a MOSFET switch and connecting the  $\overline{\text{ZERO}}$  pin to ground. This provides an active low output that may be used to control an external mute circuit, or as a logic indicator for an audio DSP/decoder or microprocessor.

## AUDIO SERIAL INTERFACE

The PCM1740 includes a three-wire serial audio interface. This includes LRCK (pin 19), BCK (pin 17), and DATA (pin 18). The LRCK input is the audio left/right clock, which is used as a latch signal for the interface. The BCK input is used to clock audio data into the serial port. The DATA input carries multiplexed data for the left and right audio channels. Audio data must be Two's Complement, MSB first formatted. Figure 8 shows the typical connection between the PCM1740 audio serial interface and an audio DSP or decoder.

## LRCK and BCK Rates

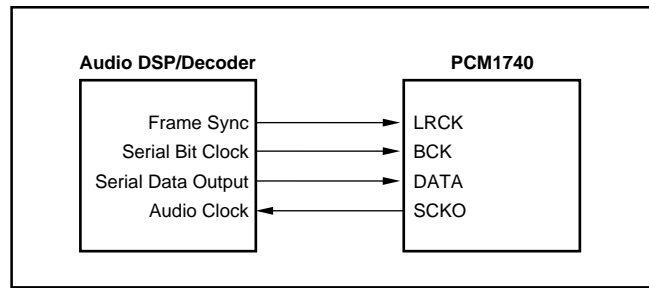


FIGURE 8. Interfacing the PCM1740 to an Audio DSP.

The LRCK input is operated at the sampling frequency,  $f_s$ . The BCK input is operated at 32, 48, or 64 times the sampling frequency. Both LRCK and BCK must be synchronous with the SCKO output for proper operation.

## Data Formats

The PCM1740 supports two audio interface formats: Standard and I<sup>2</sup>S. These formats are shown in Figure 9. The audio data word length for the Left and Right channels may be 16-, 20-, or 24-bits. The audio data word length and format are programmed using Control Registers 2 and 3. The reset default condition is Standard format with 16-bit audio data.

## Timing Requirements

Figure 10 shows the audio interface timing requirements.

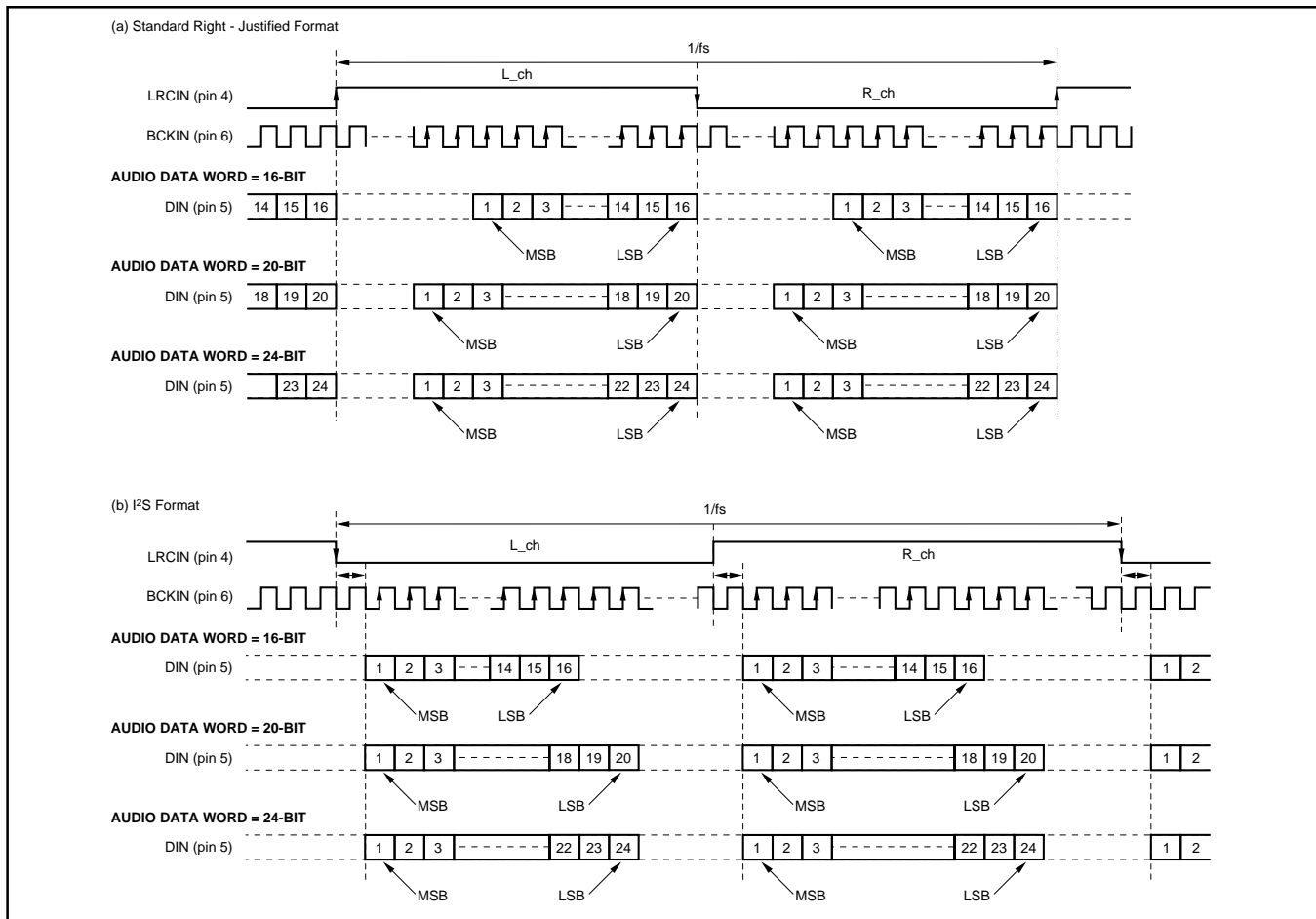


FIGURE 9. Audio Interface Formats.

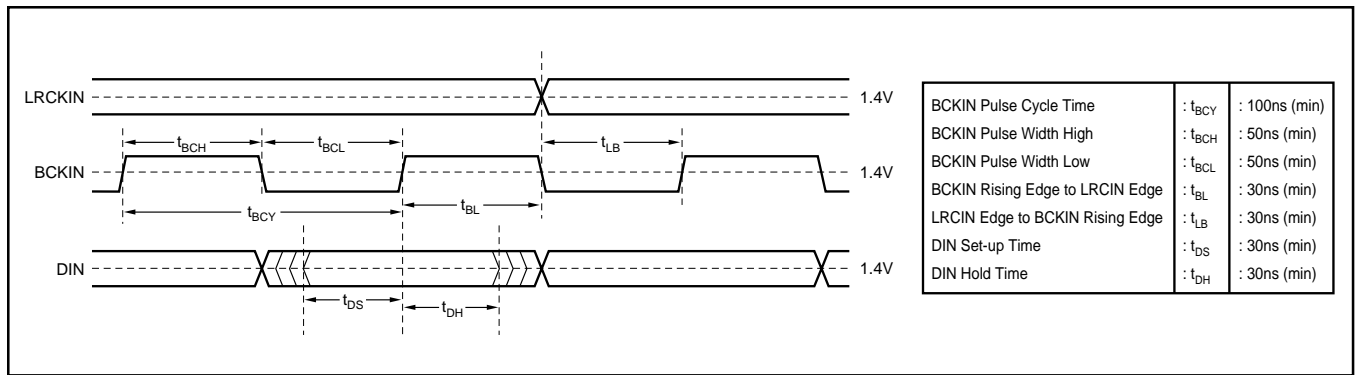


FIGURE 10. Audio Interface Timing.

### Loss of Synchronization

Ideally, LRCK and BCK will be derived from the SCKO output, ensuring synchronous operation. For other cases, the PCM1740 includes circuitry to detect loss of synchronization between the LRCK and the system clock, SCKO. A loss of synchronization condition is detected when the phase relationship between SCKO and LRCK exceeds  $\pm 6$  BCK cycles during one sample period, or  $1/f_s$ . If a loss of synchronization condition is detected, the DAC operation will halt within one sample period and the analog outputs will be forced to  $V_{CC}/2$  until re-synchronization between LRCK and SCKO is completed. Figure 11 shows the state of the analog outputs given a loss of synchronization event. During the undefined states, as well as transitions between normal and undefined states, the analog outputs may generate audible noise.

### USER PROGRAMMABLE FUNCTIONS

The PCM1740 includes a number of programmable functions, which are configured using five control registers. These registers are accessed using the I<sup>2</sup>C-Bus interface.

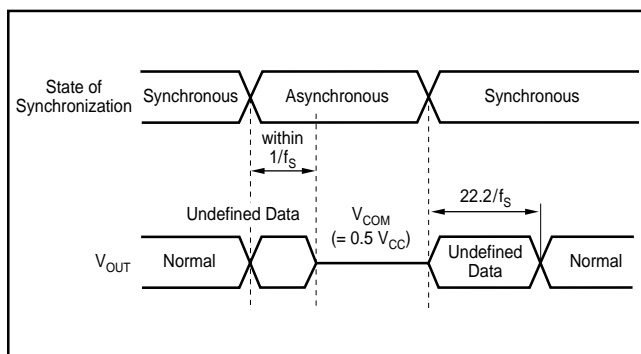


FIGURE 11. Loss of Synchronization and Analog Output State.

This section describes the control registers, while the I<sup>2</sup>C-Bus interface is described in a later section. Table II lists the available functions and their corresponding reset default condition.

### Register Map

The control register map is shown in Table III. Sub-address bits B8 through B10 are used to specify the register that is being written. All reserved bits, shown as “res”, must be set to ‘0’.

### Register Descriptions

The following pages provide detailed descriptions of the five control registers and their associated functions. All reserved bits, shown as “res”, must be set to ‘0’.

| FUNCTION  | MODE BY DEFAULT                          |
|---|--|
| Audio Data Format Select:<br>Standard Format/PS Format                | Standard Format                          |
| Audio Data Word Select:<br>16-Bit/20-Bit/24-Bit                       | 16-Bit                                   |
| Polarity of LR-clock Selection  | Left/Right = HIGH/LOW                    |
| De-emphasis Control:<br>OFF, 32kHz, 44.1kHz, 48kHz                    | OFF                                      |
| Soft Mute Control   | OFF                                      |
| Attenuation Data for Left-channel                                     | 0dB                                      |
| Attenuation Data for Right-channel                                    | 0dB                                      |
| Attenuation Data Mode Control   | Left-channel, Right-channel Individually |
| Analog Output Mode Select   | Stereo Mode                              |
| Infinity Zero Detect Mute Control                                     | OFF                                      |
| DACs Operation Control  | ON                                       |
| System Clock Select: 256f <sub>s</sub> /384f <sub>s</sub>             | 384f <sub>s</sub>                        |
| Sampling Frequency Select:<br>32kHz Group, 44.1kHz Group, 48kHz Group | 44.1kHz Group                            |
| Sampling Frequency Multiplier:<br>Normal/Double/Half                  | Normal, x1                               |

TABLE II. User-Programmable Functions.

| REGISTER   | SUB ADDRESS BYTE |     |     |     |     |     |    |    | DATA BYTE |     |      |      |     |     |     |     |
|------------|------------------|-----|-----|-----|-----|-----|----|----|-----------|-----|------|------|-----|-----|-----|-----|
|            | B15              | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7        | B6  | B5   | B4   | B3  | B2  | B1  | B0  |
| Register 0 | res              | res | res | res | res | A2  | A1 | A0 | AL7       | AL6 | AL5  | AL4  | AL3 | AL2 | AL1 | AL0 |
| Register 1 | res              | res | res | res | res | A2  | A1 | A0 | AR7       | AR6 | AR5  | AR4  | AR3 | AR2 | AR1 | AR0 |
| Register 2 | res              | res | res | res | res | A2  | A1 | A0 | PL3       | PL2 | PL1  | PL0  | IW1 | IW0 | DEM | MUT |
| Register 3 | res              | res | res | res | res | A2  | A1 | A0 | SF1       | SF0 | DSR1 | DSR0 | SYS | ATC | LRP | IIS |
| Register 4 | res              | res | res | res | res | A2  | A1 | A0 | res       | res | res  | res  | res | OPE | IZD | LD  |

TABLE III. Control Register Map.

## REGISTER DEFINITIONS

|            | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0  |
|------------|-----|-----|-----|-----|-----|-----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| Register 0 | res | res | res | res | res | 0   | 0  | 0  | AL7 | AL6 | AL5 | AL4 | AL3 | AL2 | AL1 | AL0 |

### Left Channel Attenuation Data

Default: AL[7:0] = FF<sub>HEX</sub>

Register 0 is used to set the digital attenuation level for the Left Channel. If the ATC bit in Register 3 is set to “1”, then this data is also used to control the Right Channel attenuation. The attenuation level is defined by the following relationships:

Attenuation (dB) = 20 x log (AL[7:0]<sub>DEC</sub> ÷ 256), when AL[7:0] = 01<sub>HEX</sub> (1<sub>DEC</sub>) through FE<sub>HEX</sub> (254<sub>DEC</sub>)

Attenuation (dB) = -∞ (or Mute), when AL[7:0] = 00<sub>HEX</sub>

Attenuation (dB) = 0dB, when AL[7:0] = FF<sub>HEX</sub>

The Attenuation Load bit, LD, in Register 4 must be set to “1” in order to update attenuation settings.

If LD is set to “0”, the attenuation remains at the previously programmed level, ignoring the new data until LD is set to “1”.

|            | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0  |
|------------|-----|-----|-----|-----|-----|-----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| Register 1 | res | res | res | res | res | 0   | 0  | 1  | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 |

### Right Channel Attenuation Data

Default: AR[7:0] = FF<sub>HEX</sub>

Register 1 is used to set the digital attenuation level for the Right Channel. If the ATC bit in Register 3 is set to ‘1’, then the Left Channel attenuation data in Register 1 is used to control the Right Channel attenuation. The attenuation level is defined by the following relationships:

Attenuation (dB) = 20 x log (AR[7:0]<sub>DEC</sub> ÷ 256), when AR[7:0] = 01<sub>HEX</sub> (1<sub>DEC</sub>) through FE<sub>HEX</sub> (254<sub>DEC</sub>)

Attenuation (dB) = -∞ (or Mute), when AR[7:0] = 00<sub>HEX</sub>

Attenuation (dB) = 0dB, when AR[7:0] = FF<sub>HEX</sub>

The Attenuation Load bit, LD, in Register 4 must be set to 1 in order to update attenuation settings.

If LD is set to “0”, the attenuation remains at the previously programmed level, ignoring the new data until LD is set to “1”.

|            | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0  |
|------------|-----|-----|-----|-----|-----|-----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| Register 2 | res | res | res | res | res | 0   | 1  | 0  | PL3 | PL2 | PL1 | PL0 | IW1 | IW0 | DEM | MUT |

### MUT Soft Mute Control

The MUT bit controls the soft mute function. Soft mute changes the digital attenuation level for both the Left and Right channels, stepping from the currently programmed value to infinite attenuation one step per sample period, or 1/f<sub>s</sub>. This provides a quiet muting of the outputs without audible noise.

MUT = 0      Soft Mute Disabled (default)

MUT = 1      Soft Mute Enabled

### DEM Digital De-Emphasis

The DEM bit controls the digital de-emphasis function, which is valid only for 32kHz, 44.1kHz, and 48kHz sampling frequencies. The de-emphasis plots are shown in the Typical Performance Curves section of this data sheet.

DEM = 0      De-Emphasis OFF (default)

DEM = 1      De-Emphasis ON

**IW0**  
**IW1**      **Audio Data Word Length**

The IW0 and IW1 bits are used to select the data word length for the audio serial interface. The audio data format is selected using the IIS bit in Register 3.

| IW1 | IW0 | Word Length       |
|-----|-----|-------------------|
| 0   | 0   | 16-bits (default) |
| 0   | 1   | 20-bits           |
| 1   | 0   | 24-bits           |
| 1   | 1   | Reserved          |

**PL[3:0]**      **Analog Output Mode Select**

Bits PL[3:0] are used to set the output mode for the analog outputs. Refer to the table below.

| PL3 | PL2 | PL1 | PL0 | V <sub>OUTL</sub> | V <sub>OUTR</sub> | Notes            |
|-----|-----|-----|-----|-------------------|-------------------|------------------|
| 0   | 0   | 0   | 0   | Mute              | Mute              | Mute             |
| 0   | 0   | 0   | 1   | Left              | Mute              |                  |
| 0   | 0   | 1   | 0   | Right             | Mute              |                  |
| 0   | 0   | 1   | 1   | (L+R)/2           | Mute              |                  |
| 0   | 1   | 0   | 0   | Mute              | Left              |                  |
| 0   | 1   | 0   | 1   | Left              | Left              |                  |
| 0   | 1   | 1   | 0   | Right             | Left              | Reverse          |
| 0   | 1   | 1   | 1   | (L+R)/2           | Left              |                  |
| 1   | 0   | 0   | 0   | Mute              | Right             |                  |
| 1   | 0   | 0   | 1   | Left              | Right             | Stereo (default) |
| 1   | 0   | 1   | 0   | Right             | Right             |                  |
| 1   | 0   | 1   | 1   | (L+R)/2           | Right             |                  |
| 1   | 1   | 0   | 0   | Mute              | (L+R)/2           |                  |
| 1   | 1   | 0   | 1   | Left              | (L+R)/2           |                  |
| 1   | 1   | 1   | 0   | Right             | (L+R)/2           |                  |
| 1   | 1   | 1   | 1   | (L+R)/2           | (L+R)/2           | Mono             |

| Register 3 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7  | B6  | B5   | B4   | B3  | B2  | B1  | B0  |
|------------|-----|-----|-----|-----|-----|-----|----|----|-----|-----|------|------|-----|-----|-----|-----|
|            | res | res | res | res | res | 0   | 1  | 1  | SF1 | SF0 | DSR1 | DSR0 | SYS | ATC | LRP | IIS |

**IIS**      **Audio Data Format**

The IIS bit is used to select the audio data format, either Standard Right Justified or I<sup>2</sup>S.

|         |                                    |
|---------|------------------------------------|
| IIS = 0 | Standard Right Justified (default) |
| IIS = 1 | I <sup>2</sup> S                   |

**LRP**      **LRCK Polarity**

The LRP bit selects the polarity of left/right clock input (LRCK) when using the Standard Right Justified audio data format. This bit has no effect when using the I<sup>2</sup>S audio data format.

|         |  |
|---------|--|
| LRP = 0 | Left Channel when LRCK = High; Right Channel when LRCK = Low (default) |
| LRP = 1 | Left Channel when LRCK = Low; Right Channel when LRCK = High           |

**ATC**      **Attenuation Mode Control**

The ATC bit is used to select independent or common attenuation data for the Left and Right channels.

|         |   |
|---------|---|
| ATC = 0 | Independent: Left Channel uses Register 0 and Right Channel uses Register 1 (default) |
| ATC = 1 | Common: Left and Right Channels both use Register 0                                   |

## SYS Audio System Clock (or SCKO)

The SYS bit is used to select the system clock (or SCKO) frequency, either  $256f_s$  or  $384f_s$ .

|         |                    |
|---------|--------------------|
| SYS = 0 | $384f_s$ (default) |
| SYS = 1 | $256f_s$           |

## DSR0 DSR1 Sampling Frequency Multiplier

The DSR0 and DSR1 bits are used to select the multiplier used in conjunction with the SF0 and SF1 bits.

| DSR1 | DSR0 | Multiplier           |
|------|------|----------------------|
| 0    | 0    | Normal, x1 (default) |
| 0    | 1    | Double, x2           |
| 1    | 0    | Half, x 1/2          |
| 1    | 1    | Reserved             |

## SF0 Sampling Frequency Select

SF1 The SF0 and SF1 bits are used to select the sampling frequency group (32kHz, 44.1kHz, or 48kHz). The DSR0 and DSR1 bits, described previously, are used to select the multiplier.

| SF1 | SF0 | Sampling Frequency Group                                 |
|-----|-----|--|
| 0   | 0   | 44.1kHz Group ( 22.05kHz, 44.1kHz, or 88.2kHz) (default) |
| 0   | 1   | 48 kHz Group (24kHz, 48kHz, or 96kHz)                    |
| 1   | 0   | 32 kHz Group (16kHz, 32kHz, or 64kHz)                    |
| 1   | 1   | Reserved   |

| Register 4 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0 |
|------------|-----|-----|-----|-----|-----|-----|----|----|-----|-----|-----|-----|-----|-----|-----|----|
|            | res | res | res | res | res | 1   | 0  | 0  | res | res | res | res | res | OPE | IZD | LD |

## LD Attenuation Data Load Control

The LD bit is used to simultaneously set the Left and Right digital attenuation data. When LD is set to “1”, the digital attenuation data given by Registers 0 and 1 is loaded for the Left and Right channels. When LD is set to “0”, updates to Registers 0 and 1 are ignored, and the attenuation settings remain as previously programmed until LD is set to “1”.

|        |   |
|--------|---|
| LD = 0 | Disabled  |
| LD = 1 | Enabled: Left and Right Attenuation Data Updated Simultaneously |

## IZD Infinite Zero Detect Mute

The IZD bit is used to enable/disable the infinite zero detect mute function. The PCM1740 includes infinite zero detection logic that monitors the audio data at the DATA input (pin 18). If the audio data for both the Left and Right channels is all zeros for 65,536 continuous BCK clock cycles, the zero flag will be activated and output amplifier will be disconnected from the output of the delta-sigma modulator. The output amplifier’s input is switched to the DC common mode voltage. This forces  $V_{OUTL}$  and  $V_{OUTR}$  to  $V_{CC}/2$ . The  $\overline{ZERO}$  output flag (pin 16) is not affected by the setting of this bit.

|         |                    |
|---------|--------------------|
| IZD = 0 | Disabled (default) |
| IZD = 1 | Enabled            |

## OPE DAC Operation Control

The OPE bit is used to enable/disable the operation of the D/A converters. When enabled, the DAC outputs are connected to the output amplifier for normal operation. When disabled, the output amplifier is disconnected from the DAC output and switched to the DC common mode voltage. This forces  $V_{OUTL}$  and  $V_{OUTR}$  to  $V_{CC}/2$ .

|         |  |
|---------|--|
| OPE = 0 | Enabled: Normal Operation(default)     |
| OPE = 1 | Disabled: Outputs forced to $V_{CC}/2$ |

## I<sup>2</sup>C-BUS INTERFACE DESCRIPTION

The PCM1740 includes an I<sup>2</sup>C-Bus interface for writing the internal control registers. This provides an industry standard method for interfacing a host CPU control port to the PCM1740. The PCM1740 operates as a Slave receiver on the bus, and supports data transfer rates up to 100 kilobits-per-second (kbps).

The I<sup>2</sup>C-Bus interface is comprised of four signals: SDA (pin 9), SCL (pin 8), AD0 (pin 6), and AD1 (pin 7). The SCL input is the serial data clock, while SDA is the serial data input. SDA carries start/stop, slave address, sub-address (or register address), register, and acknowledgment data. The AD0 and AD1 inputs form the lower two bits of the slave address.

### Slave Address

The PCM1740 Slave address consists of seven bits, as shown in Figure 12. The five most significant bits are fixed, while the two least significant bits, named A0 and A1, are defined by the logic levels present at the AD0 and AD1 input pins. This allows four PCM1740s to reside on the same I<sup>2</sup>C-Bus.

## Bus Operation

Figure 13 shows the typical configuration of the PCM1740 on the I<sup>2</sup>C-Bus. The Master transmitter or transmitter/receiver is typically a microcontroller, or an audio DSP/decoder. The Master device controls the data transfers on the bus. The PCM1740 operates as a Slave receiver, and accepts data from the Master when it is properly addressed. The data transfer may be comprised of an unlimited number of bytes, or 8-bit data words. Figure 14 shows the message transfer protocol.

For normal bit transfer on the bus, data on SDA must be static while SCL is High. Data on SDA may change High/Low states when SCL is Low. The exception to this rule is the Start and Stop conditions.

The Start condition is defined by a High-to-Low transition on SDA while SCL is High, and is denoted with an  $\overline{S}$  in Figure 12. The Stop condition is defined by a Low-to-High transition on SDA while SCL is High, and is denoted with a  $\overline{P}$  in Figure 12. The Start and Stop conditions are always generated by the Master. All data transfers from Master to Slave begin with a Start condition and end with a Stop condition. The bus is considered to be busy after the Start condition, and becomes free some time after the Stop condition.

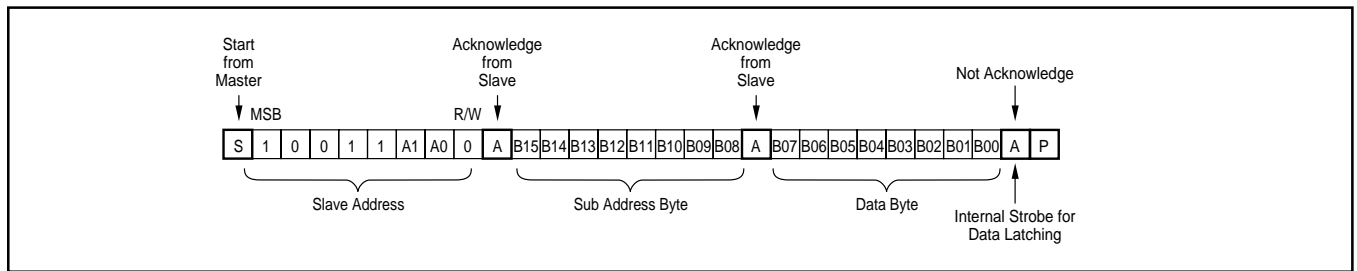


FIGURE 12. Control Data Format.

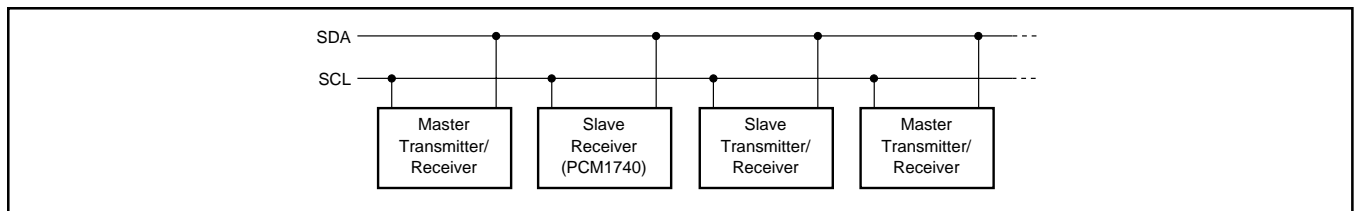
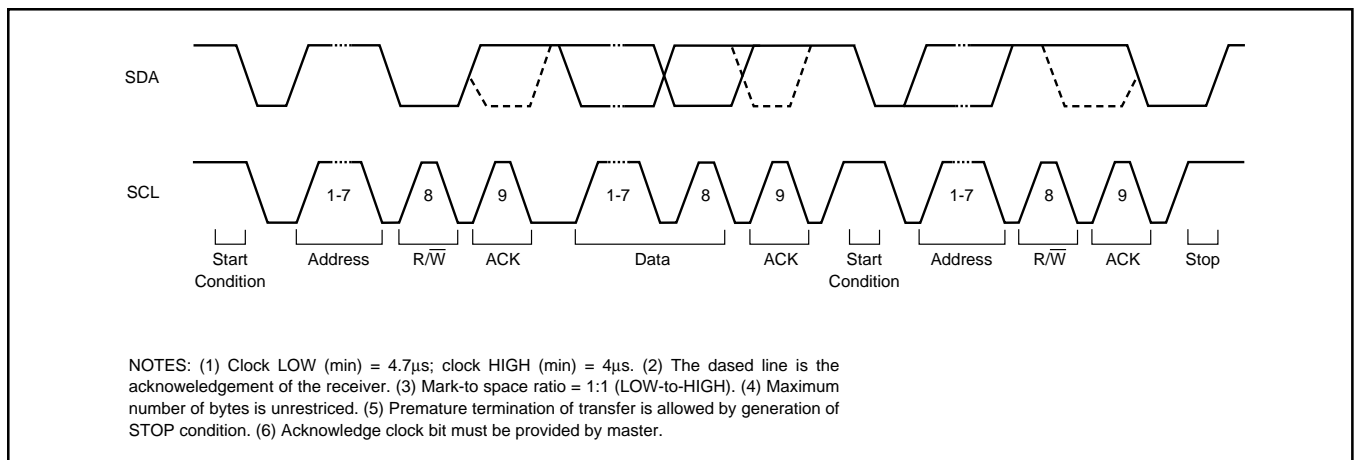


FIGURE 13. Typical I<sup>2</sup>C-Bus Configuration.



NOTES: (1) Clock LOW (min) = 4.7 $\mu$ s; clock HIGH (min) = 4 $\mu$ s. (2) The dashed line is the acknowledgement of the receiver. (3) Mark-to space ratio = 1:1 (LOW-to-HIGH). (4) Maximum number of bytes is unrestricted. (5) Premature termination of transfer is allowed by generation of STOP condition. (6) Acknowledge clock bit must be provided by master.

FIGURE 14. I<sup>2</sup>C Bus Data Transfer.

Data transfer begins with a Start condition, and is immediately followed by the Slave address and Read/Write bit. The Read/Write bit is set to “0” for the PCM1740, in order to write data to the control register specified by the sub-address. This is followed by an acknowledgment from the PCM1740, the sub-address (i.e., control register address), another acknowledgment from the PCM1740, the control register data, and another acknowledgment from the PCM1740. What happens after this depends upon if the user wants to continue writing additional control registers, or if they want to terminate the data transfer. If the user wants to continue, the acknowledgment is followed by a Start condi-

tion for the next write sequence. If the user decides to terminate the data transfer, then a Stop condition is generated by the Master.

The I<sup>2</sup>C-Bus specification defines timing requirements for devices connected to the bus. Timing requirements for the PCM1740 are shown in Figure 15.

### Reference

For additional information regarding the I<sup>2</sup>C-Bus, please refer to the I<sup>2</sup>C-Bus Specification, Version 2.0, published in December 1998 by Philips Semiconductors.

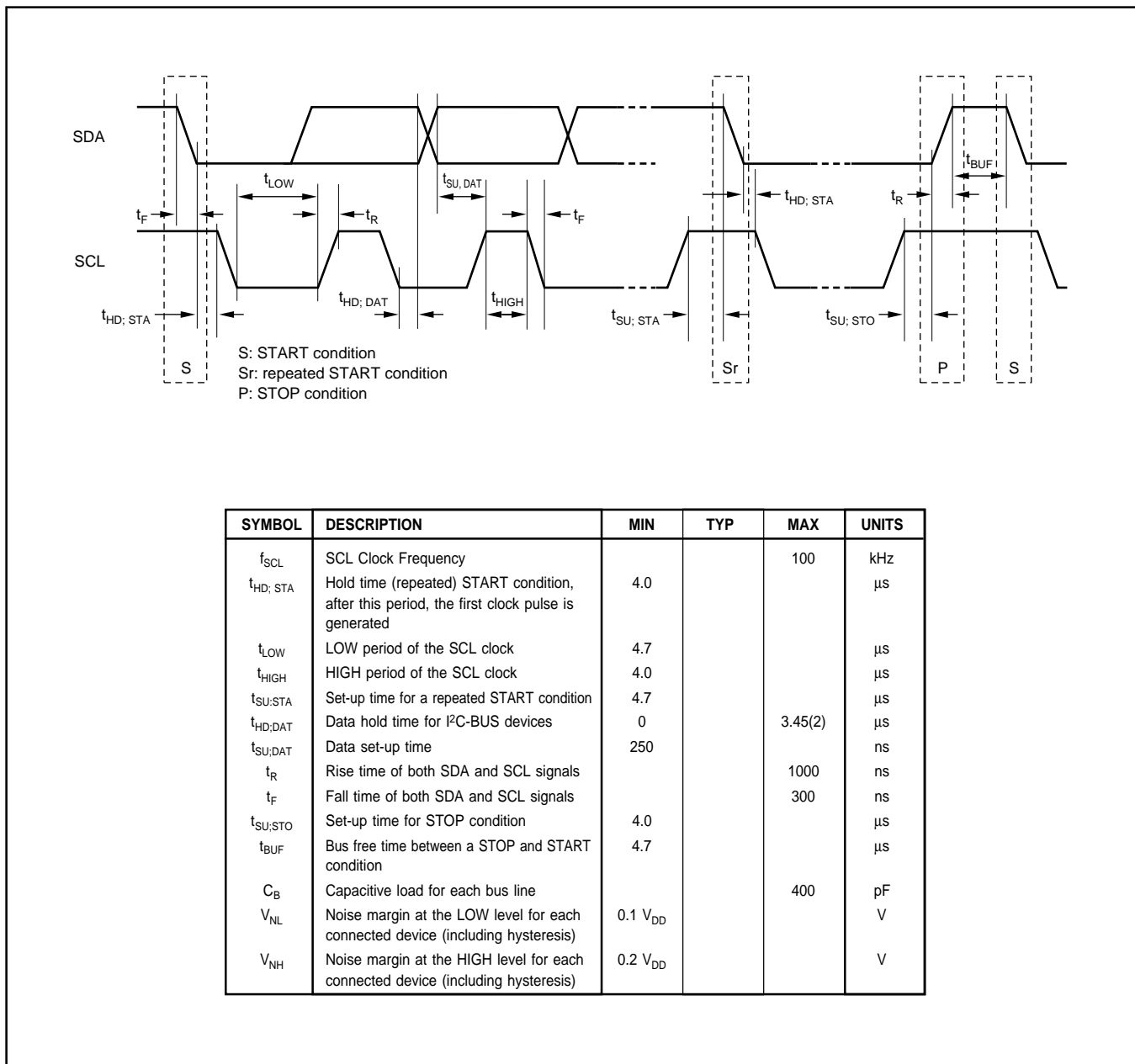


FIGURE 15. I<sup>2</sup>C Bus Timing.



## APPLICATIONS INFORMATION

### Basic Connection Diagram

A basic connection diagram is shown in Figure 16. Power supply and reference de-coupling capacitors should be located as close as possible to the PCM1740 package. The 27MHz crystal should also be located as close as possible to the package, to reduce the effects of parasitic capacitance on VCXO operation.

A single +5V supply is recommended, to avoid issues with power-supply sequencing and SCR latch-up. It is recommended that this supply be separate from the system's digital power supply. In cases where this is not practical, an

inductor or ferrite bead should be placed in series with the +5V supply connection to reduce or eliminate high-frequency noise on the supply line.

In cases where overshoot or ringing is present on the LRCK or BCK signals, a series resistance of 25Ω to 100Ω should be added. The resistor forms a simple RC filter with the device input and PCB parasitic capacitance, dampening the overshoot and ringing effects, while reducing high-frequency noise emissions.

### Typical Application Diagram

Figure 17 shows the PCM1740 being used as part of the audio sub-system in a set-top box application.

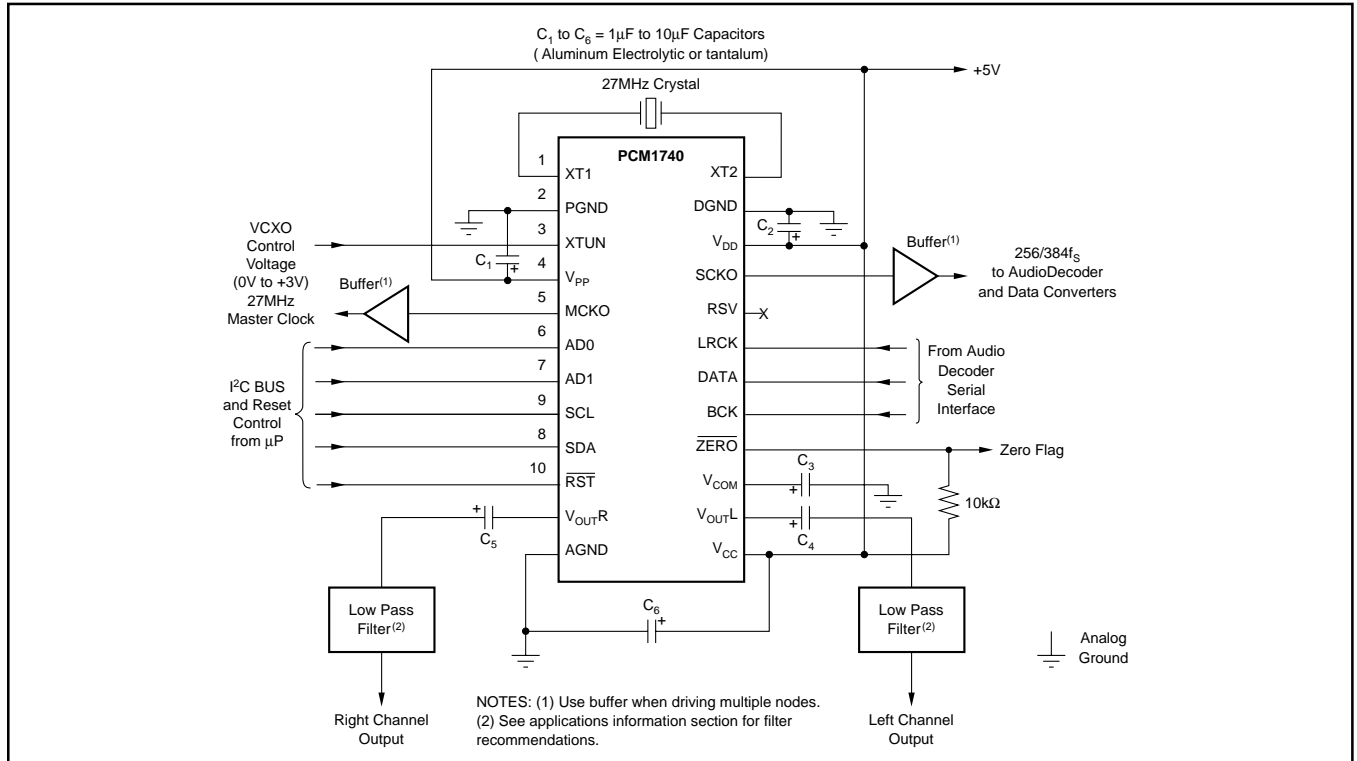


FIGURE 16. Basic Connection Diagram.

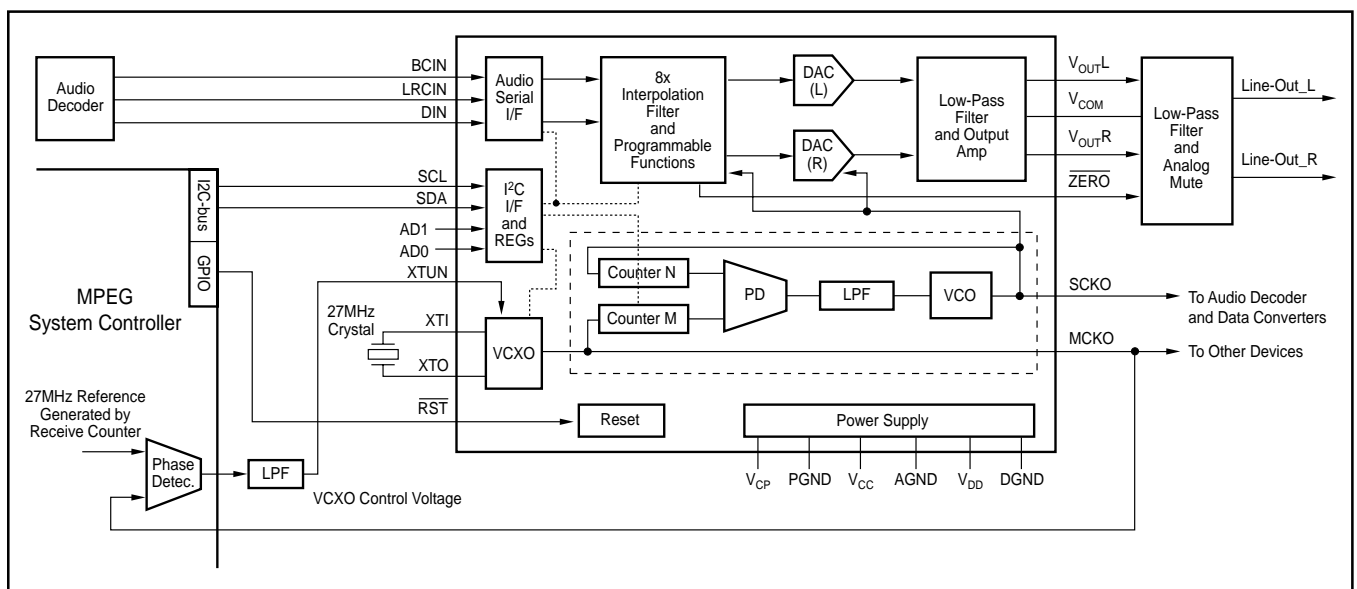


FIGURE 17. Typical Application Diagram.

The VTUN control voltage is generated by the MPEG-2 controller, which compares the MCKO output clock from the PCM1740 with the clock count received from the transmitter. VTUN is adjusted to retain clock synchronization between the transmitted and received signals. The SCKO output is used as the audio master clock for the audio decoder and additional data converters.

### V<sub>COM</sub> Output

The unbuffered DC common-mode voltage output, V<sub>COM</sub> (pin 15), is brought out mainly for de-coupling purposes. V<sub>COM</sub> is nominally biased to V<sub>CC</sub>/2. The V<sub>COM</sub> output may be used to bias external circuits, but it must be connected to a high-impedance node or buffered using a voltage follower.

Figure 18 shows examples of the proper use of the V<sub>COM</sub> output for external biasing applications.

### DAC Output Filtering

Delta-Sigma D/A converters utilize noise shaping techniques to improve in-band signal-to-noise (SNR) performance at the expense of generating increased out of band noise above the Nyquist frequency, or f<sub>S</sub>/2. The out of band noise must be low-pass filtered in order to provide optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

The PCM1740 includes an on-chip low-pass filter as part of the output amplifier stage. The frequency response for the filter is shown in the Typical Performance Curves section of this data sheet. The -3dB cutoff frequency is fixed at 100kHz.

Figure 19 shows the recommended external low-pass active filter circuits for dual and single-supply applications. These circuits are second-order Butterworth filters using the Multiple Feedback (MFB) circuit arrangement. Both filters have a cutoff frequency of 30kHz. Figure 19(a) is a dual-supply filter with a gain of 1.85 (for a standard 2 V<sub>RMS</sub> line output level). Figure 19(b) is a single-supply filter with a gain of 1. Values for the filter components may be calculated using the FilterPro program, available from the Burr-Brown web site ([www.burr-brown.com](http://www.burr-brown.com)) and local sales offices. For more information regarding MFB active filter design and the FilterPro program, please refer to Burr-Brown Applications Bulletin, AB-034.

Since the overall system performance is defined primarily by the quality of the D/A converters and their associated analog output circuitry, op amps designed specifically for audio applications are recommended for the active filters. Burr-Brown's OPA2134, OPA2353, and OPA2343 dual op amps are ideal for use with the PCM1740.

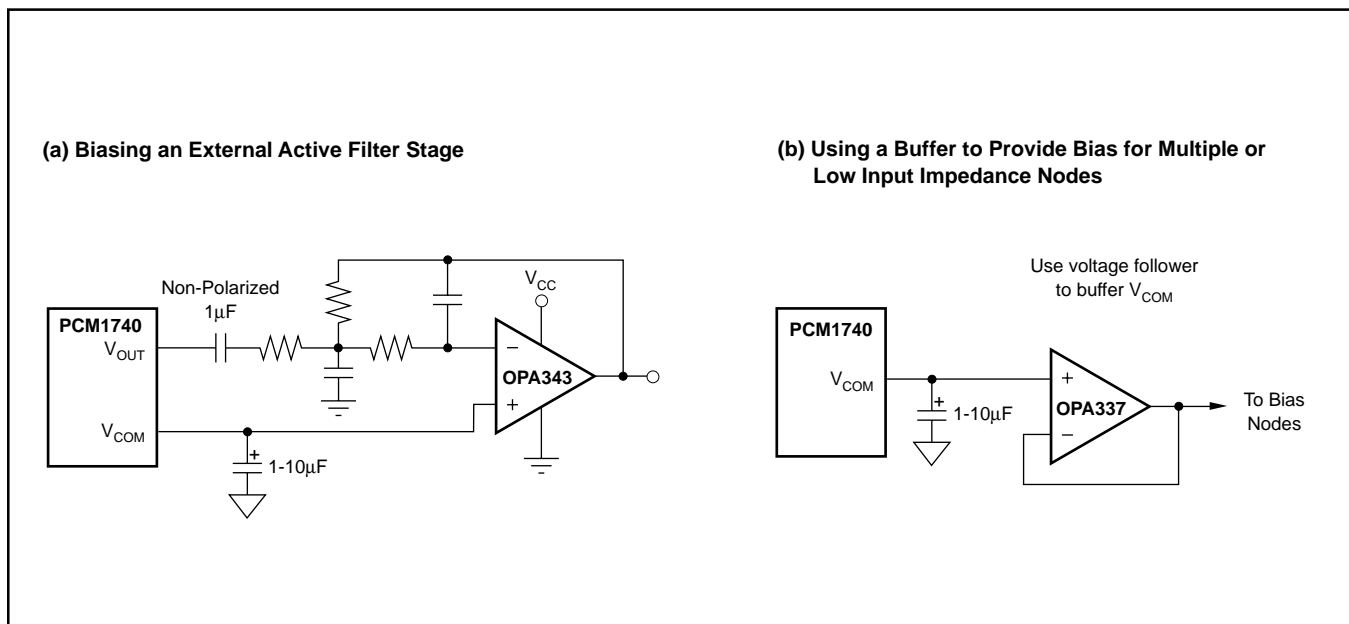
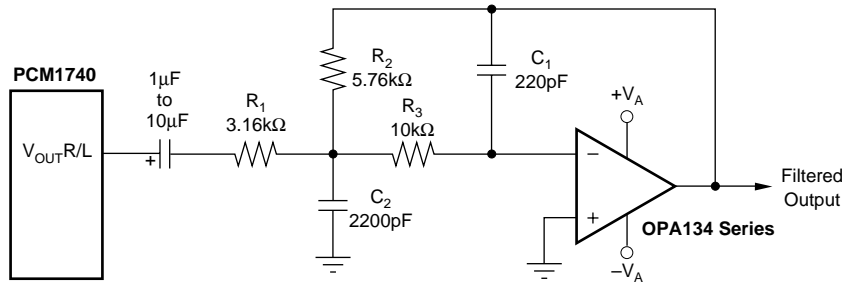
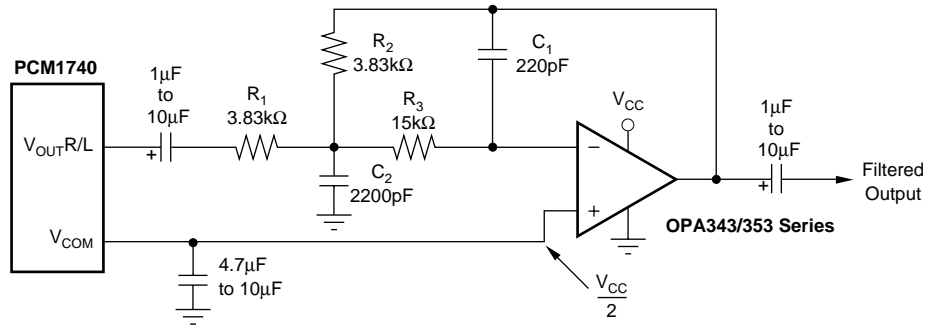


FIGURE 18. Using V<sub>COM</sub> To Bias External Circuitry.



(a) Dual-Supply Filter Circuit



(b) Single-Supply Filter Circuit

FIGURE 19. Recommended Output Filter Circuits.

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| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| PCM1740E         | ACTIVE                | SSOP         | DB              | 24   | 58          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCM1740E/2K      | ACTIVE                | SSOP         | DB              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCM1740E/2KG4    | ACTIVE                | SSOP         | DB              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

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<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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| Data Converters  | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>     | Automotive          | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>         |
| DSP              | <a href="http://dsp.ti.com">dsp.ti.com</a>                         | Broadband           | <a href="http://www.ti.com/broadband">www.ti.com/broadband</a>           |
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