

# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA and LTE base station applications with frequencies from 2110 to 2170 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ} = 700$  mA,  $P_{out} = 24$  Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	17.9	33.0	6.4	-38.7
2140 MHz	18.1	33.0	6.4	-38.2
2170 MHz	18.3	33.4	6.3	-37.2

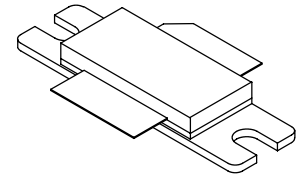
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 2140 MHz, 138 Watts CW <sup>(1)</sup> Output Power (3 dB Input Overdrive from Rated  $P_{out}$ )
- Typical  $P_{out}$  @ 1 dB Compression Point  $\approx$  100 Watts CW

### Features

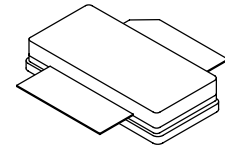
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units, 56 mm Tape Width, 13 inch Reel. For R5 Tape and Reel option, see p. 14.

**MRF8S21100HR3**  
**MRF8S21100HSR3**

**2110-2170 MHz, 24 W AVG., 28 V**  
**W-CDMA, LTE**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**CASE 465-06, STYLE 1**  
**NI-780**  
**MRF8S21100HR3**



**CASE 465A-06, STYLE 1**  
**NI-780S**  
**MRF8S21100HSR3**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature <sup>(2,3)</sup>	$T_J$	225	°C
CW Operation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	CW	108 0.57	W W/°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value <sup>(3,4)</sup>	Unit
Thermal Resistance, Junction to Case Case Temperature 77°C, 24 W CW, 28 Vdc, $I_{DQ} = 700$ mA, 2140 MHz Case Temperature 80°C, 100 W CW <sup>(1)</sup> , 28 Vdc, $I_{DQ} = 700$ mA, 2140 MHz	$R_{\theta JC}$	0.48 0.45	°C/W

1. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
2. Continuous use at maximum temperature will affect MTTF.
3. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
4. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 150\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_D = 700\ \text{mAdc}$ )	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage <sup>(1)</sup> ( $V_{DD} = 28\text{ Vdc}$ , $I_D = 700\ \text{mAdc}$ , Measured in Functional Test)	$V_{GG(Q)}$	4.0	5.4	7.0	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1.5\ \text{Adc}$ )	$V_{DS(on)}$	0.1	0.24	0.3	Vdc

**Functional Tests** <sup>(2)</sup> (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 700\ \text{mA}$ ,  $P_{out} = 24\ \text{W Avg.}$ ,  $f = 2170\ \text{MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\ \text{MHz}$  Offset.

Power Gain	$G_{ps}$	17.2	18.3	20.2	dB
Drain Efficiency	$\eta_D$	31.0	33.4	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.9	6.3	—	dB
Adjacent Channel Power Ratio	ACPR	—	-37.2	-36.0	dBc
Input Return Loss	IRL	—	-12	-7	dB

**Typical Broadband Performance** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 700\ \text{mA}$ ,  $P_{out} = 24\ \text{W Avg.}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\ \text{MHz}$  Offset.

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	17.9	33.0	6.4	-38.7	-18
2140 MHz	18.1	33.0	6.4	-38.2	-16
2170 MHz	18.3	33.4	6.3	-37.2	-12

- $V_{GG} = 2 \times V_{GS(Q)}$ . Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
- Part internally matched both on input and output.

(continued)

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Typical Performance</b> (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28$ Vdc, $I_{DQ} = 700$ mA, 2110-2170 MHz Bandwidth					
$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	100	—	W
IMD Symmetry @ 36 W PEP, $P_{out}$ where IMD Third Order Intermodulation $\cong 30$ dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD <sub>sym</sub>	—	40	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW <sub>res</sub>	—	50	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 24$ W Avg.	$G_F$	—	0.4	—	dB
Gain Variation over Temperature ( $-30^\circ\text{C}$ to $+80^\circ\text{C}$ )	$\Delta G$	—	0.011	—	dB/ $^\circ\text{C}$
Output Power Variation over Temperature ( $-30^\circ\text{C}$ to $+80^\circ\text{C}$ ) (1)	$\Delta P1dB$	—	0.005	—	dB/ $^\circ\text{C}$

1. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.

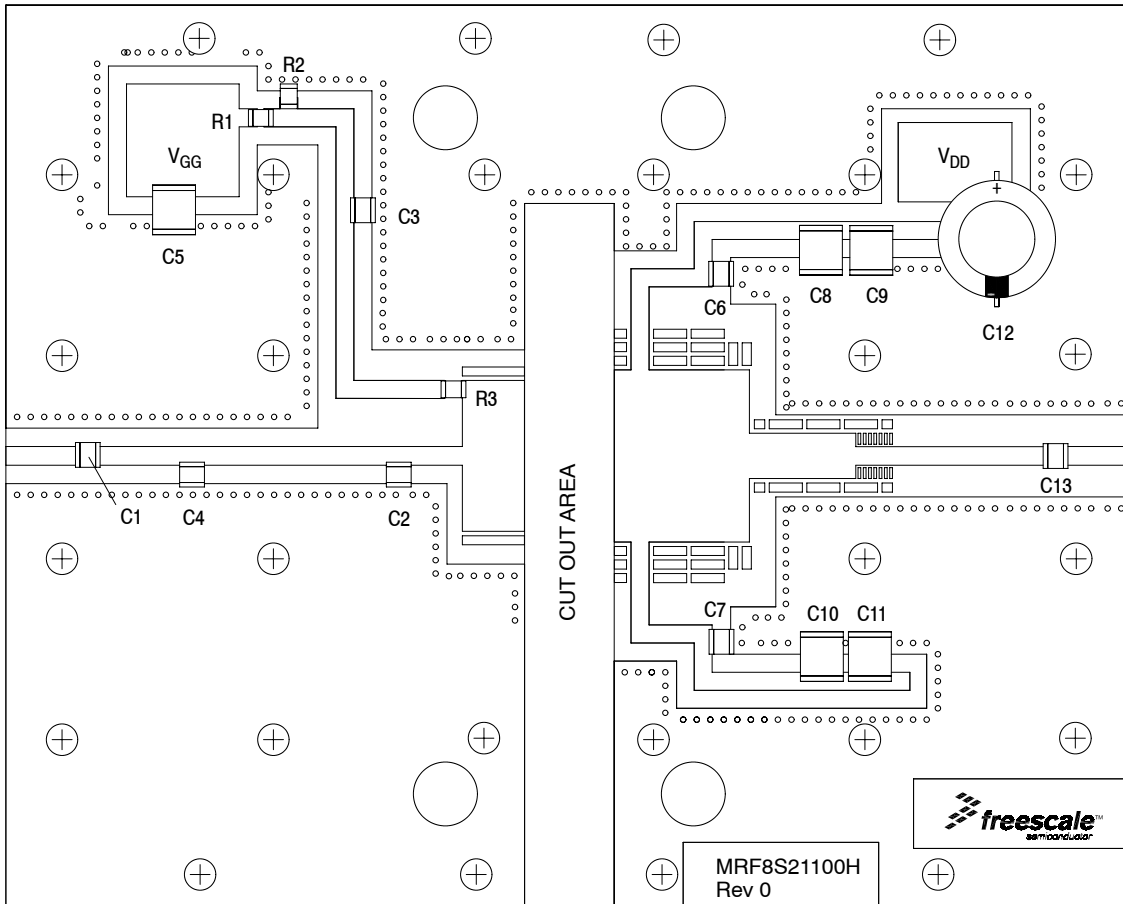
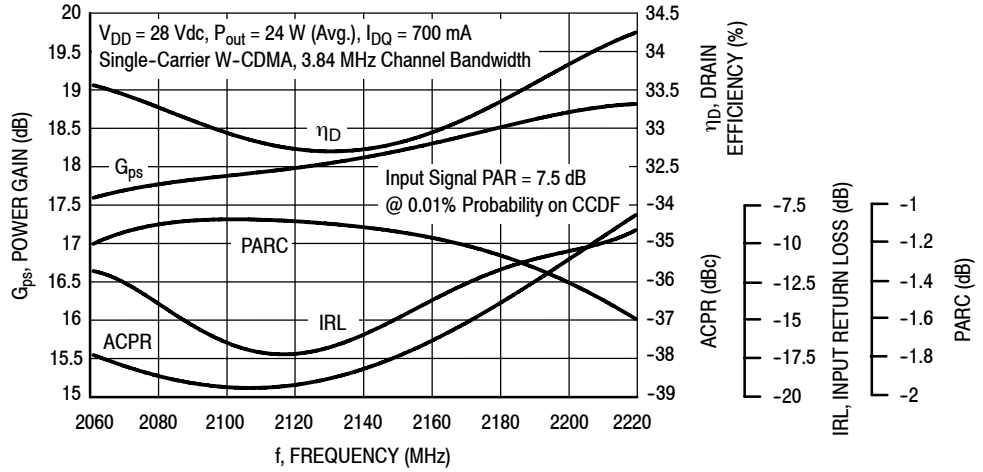


Figure 1. MRF8S21100HR3(HSR3) Test Circuit Component Layout

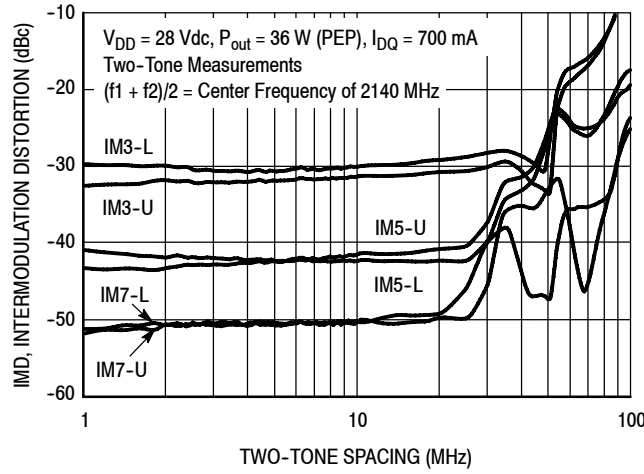
Table 5. MRF8S21100HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C3, C6, C7	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C2	1.6 pF Chip Capacitor	ATC100B1R6BT500XT	ATC
C4	0.2 pF Chip Capacitor	ATC100B0R2BT500XT	ATC
C5, C8, C9, C10, C11	10 $\mu$ F, 50 V Tantalum Capacitors	293D106X9050E2TE3	Vishay
C12	220 $\mu$ F, 50 V Electrolytic Capacitor, Radial	227CKS050M	Illinois Capacitor
C13	5.6 pF Chip Capacitor	ATC100B5R6CT500XT	ATC
R1, R2	2 K $\Omega$ , 1/4 W Chip Resistors	CRCW12062K00FKEA	Vishay
R3	10 $\Omega$ , 1/4 W Chip Resistor	CRCW120610R0JNEA	Vishay
PCB	0.030", $\epsilon_r = 2.55$	AD255A	Arlon

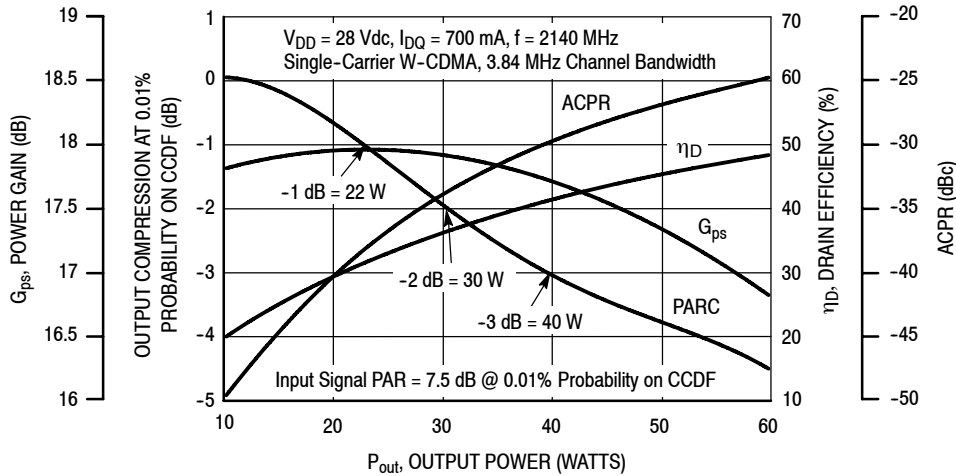
### TYPICAL CHARACTERISTICS



**Figure 2. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 24$  Watts Avg.**

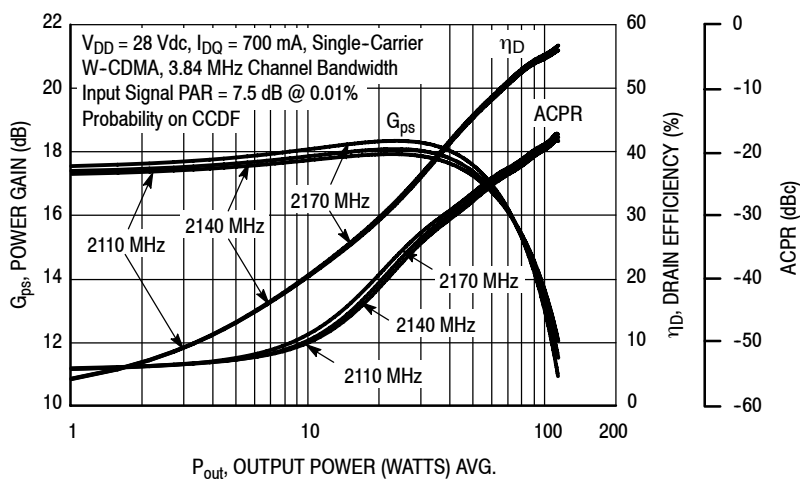


**Figure 3. Intermodulation Distortion Products versus Two-Tone Spacing**

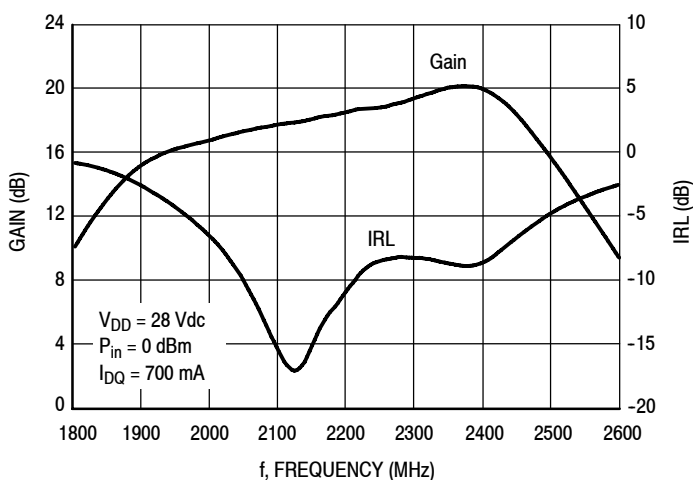


**Figure 4. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

### TYPICAL CHARACTERISTICS

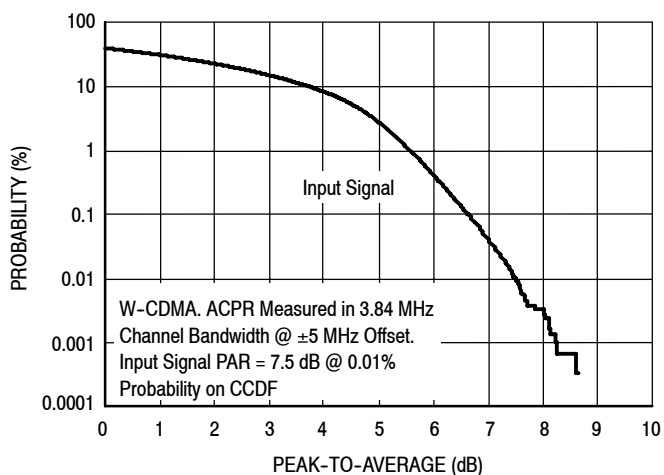


**Figure 5. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**

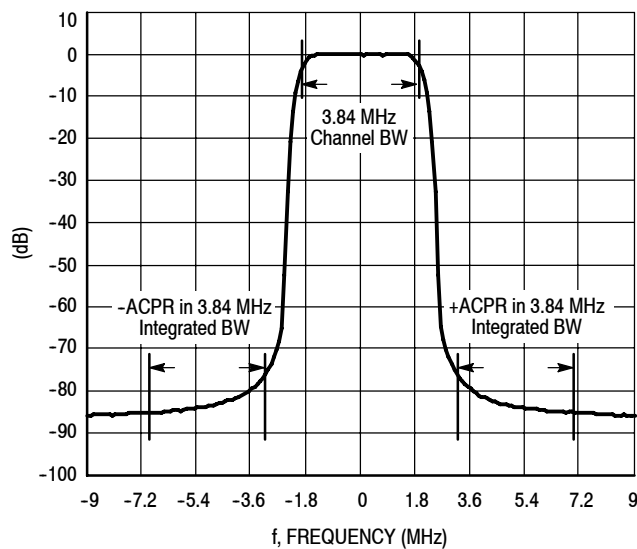


**Figure 6. Broadband Frequency Response**

### W-CDMA TEST SIGNAL



**Figure 7. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal**



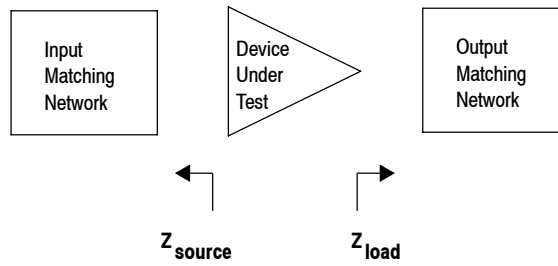
**Figure 8. Single-Carrier W-CDMA Spectrum**

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 700 \text{ mA}$ ,  $P_{out} = 24 \text{ W Avg.}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
2060	4.41 - j6.05	3.03 - j3.64
2080	4.38 - j5.67	2.96 - j3.45
2100	4.33 - j5.29	2.89 - j3.26
2120	4.33 - j4.91	2.83 - j3.10
2140	4.33 - j4.54	2.75 - j2.94
2160	4.33 - j4.17	2.69 - j2.75
2180	4.31 - j3.80	2.62 - j2.50
2200	4.32 - j3.39	2.65 - j2.24
2220	4.35 - j2.99	2.67 - j2.04

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

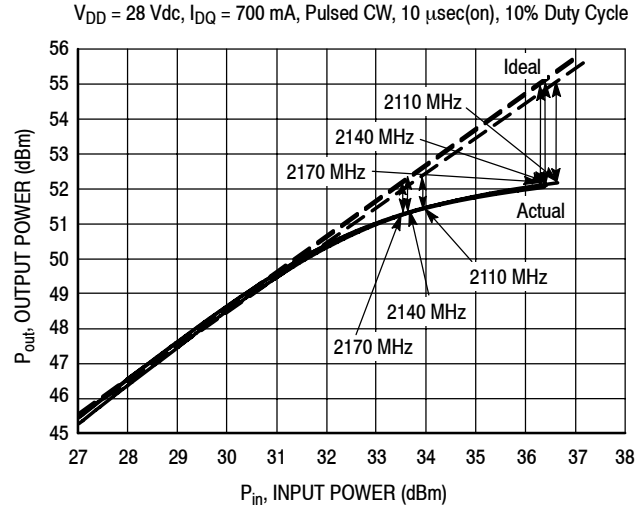
$Z_{load}$  = Test circuit impedance as measured from drain to ground.



**Figure 9. Series Equivalent Source and Load Impedance**



## ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

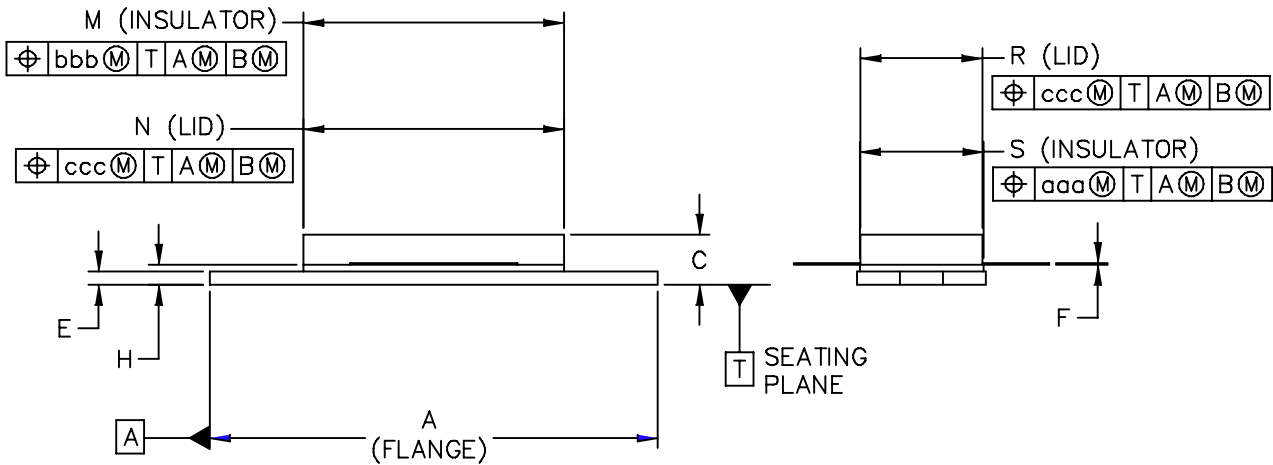
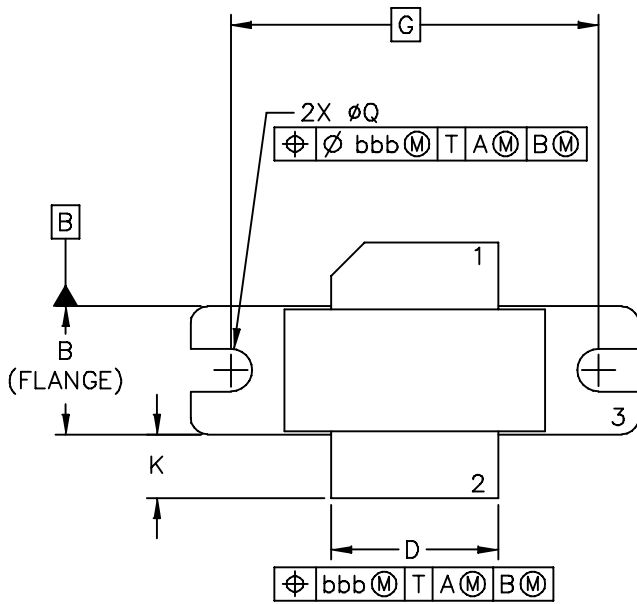
f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
2110	141	51.5	166	52.2
2140	141	51.5	162	52.1
2170	138	51.4	158	52.0

Test Impedances per Compression Level

f (MHz)		$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
2110	P1dB	$3.50 - j7.47$	$1.65 - j3.64$
2140	P1dB	$4.21 - j7.53$	$1.57 - j3.70$
2170	P1dB	$6.39 - j8.09$	$1.66 - j3.68$

**Figure 10. Pulsed CW Output Power versus Input Power @ 28 V**

PACKAGE DIMENSIONS



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	CASE NUMBER: 465-06		31 MAR 2005
	STANDARD: NON-JEDEC		

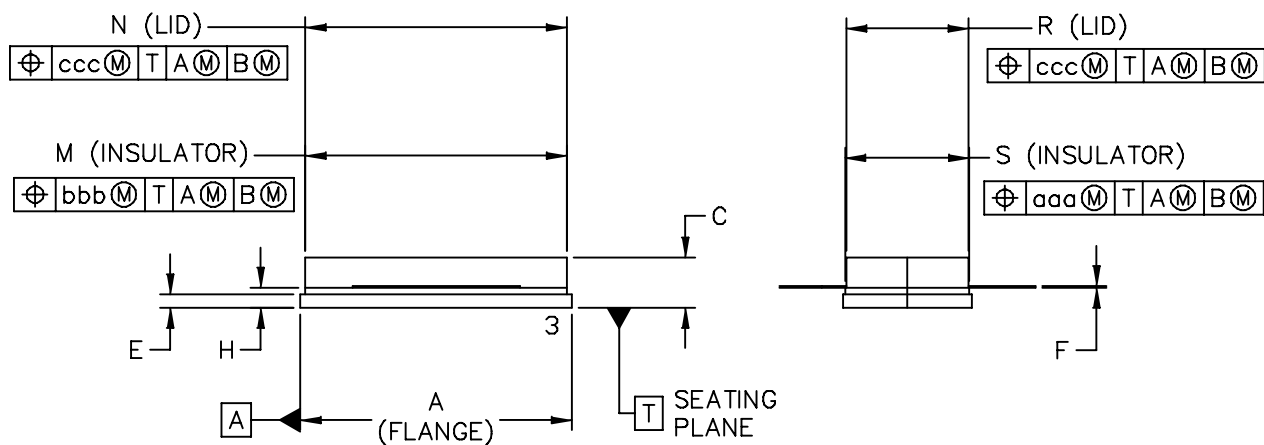
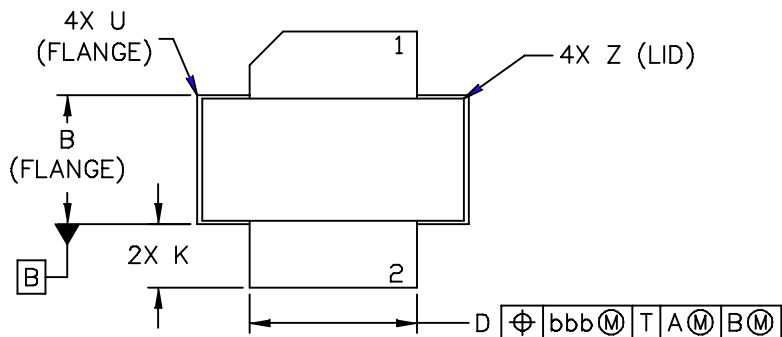
NOTES:

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2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (.762) AWAY FROM PACKAGE BODY.

STYLE 1:

- PIN 1. DRAIN  
 2. GATE  
 3. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16	R	.365	.375	9.27	9.53
B	.380	.390	9.65	9.91	S	.365	.375	9.27	9.52
C	.125	.170	3.18	4.32	aaa	—	.005	—	0.127
D	.495	.505	12.57	12.83	bbb	—	.010	—	0.254
E	.035	.045	0.89	1.14	ccc	—	.015	—	0.381
F	.003	.006	0.08	0.15	—	—	—	—	—
G	1.100 BSC		27.94 BSC		—	—	—	—	—
H	.057	.067	1.45	1.7	—	—	—	—	—
K	.170	.210	4.32	5.33	—	—	—	—	—
M	.774	.786	19.66	19.96	—	—	—	—	—
N	.772	.788	19.6	20	—	—	—	—	—
Q	∅.118	∅.138	∅3	∅3.51	—	—	—	—	—
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STYLE 1:

- PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.805	-.815	20.45	20.7	U	-.040	-	-	1.02
B	.380	-.390	9.65	9.91	Z	-.030	-	-	0.76
C	.125	-.170	3.18	4.32	aaa	-.005	-	-	0.127
D	.495	-.505	12.57	12.83	bbb	-.010	-	-	0.254
E	.035	-.045	0.89	1.14	ccc	-.015	-	-	0.381
F	.003	-.006	0.08	0.15	-	-	-	-	-
H	.057	-.067	1.45	1.7	-	-	-	-	-
K	.170	-.210	4.32	5.33	-	-	-	-	-
M	.774	-.786	19.61	20.02	-	-	-	-	-
N	.772	-.788	19.61	20.02	-	-	-	-	-
R	.365	-.375	9.27	9.53	-	-	-	-	-
S	.365	-.375	9.27	9.52	-	-	-	-	-

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		STANDARD: NON-JEDEC			

## PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents, tools and software to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

## R5 TAPE AND REEL OPTION

R5 Suffix = 50 Units, 56 mm Tape Width, 13 inch Reel.

The R5 tape and reel option for MRF8S21100H and MRF8S21100HS parts will be available for 2 years after release of MRF8S21100H and MRF8S21100HS. Freescale Semiconductor, Inc. reserves the right to limit the quantities that will be delivered in the R5 tape and reel option. At the end of the 2 year period customers who have purchased these devices in the R5 tape and reel option will be offered MRF8S21100H and MRF8S21100HS in the R3 tape and reel option.

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2010	• Initial Release of Data Sheet
1	Mar. 2011	• Corrected $V_{GG(Q)} V_{DD}$ value from 30 Vdc to 28 Vdc in On Characteristics table to reflect actual test measurement condition, p. 2

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Technical Information Center  
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### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor China Ltd.  
Exchange Building 23F  
No. 118 Jianguo Road  
Chaoyang District  
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China  
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